INSTRUCTION MANUAL FOR THE MODEL 610D/OPTION 16 SWEEP GENERATOR GENERAL PURPOSE INTERFACE BUS (GPIB)

WILTRON

INSTRUCTION MANUAL FOR THE

MODEL 610D/OPTION 16 SWEEP GENERATOR

GENERAL PURPOSE INTERFACE BUS (GPIB)

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Q.A # BOOK

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SECTION I
GENERAL INFORMATION

1-1. INTRODUCTION

This manual contains operation and maintenance information on the Option 16 General Purpose Interface Bus (GPIB) circuits of the Model 610D RF Sweep Generator. (For information on other Model 610D circuits, refer to the WILTRON Model 610D Operation and Maintenance Manual.) Section I, General Information, provides a general description of the Model 610D/ Option 16 and the IEEE 488 GPIB. Section II, Installation, is not applicable; the interface circuitry is installed at the factory, and the Model 610D/Option 16 is supplied to the customer fully-assembled. Section III, Operation, provides information regarding GPIB interface, programming instructions, and typical test setups using Tektronix, Hewlett-Packard, and Commodore control units. Section IV, Functional Description, contains circuit descriptions for the Option 16 PC assemblies. Section V, Performance Verification, contains information for testing the Option 16 circuits. Section VI, Maintenance, provides maintenance instructions, including test and adjustment data. Section VII, Parts Lists, provides parts lists, and Section VIII, Diagrams, contains the schematic diagrams and GPIB timing information.

1-2. DESCRIPTION OF MODEL 610D/OPTION 16

The Model 610D/Option 16 RF Sweep Generator conforms to the IEEE 488 and IEC 625 standards for programming instrumentation. The option provides the interface circuitry to enable the Model 610D RF Sweep Generator (with appropriate RF plug-in) to be used in an automatic measurement system. The Option 16 circuitry within the Model 610D RF Sweep Generator consists of two printed circuit (PC) assemblies and an interface connector mounted on the generator rear panel.

1-3. DESCRIPTION OF THE INTERFACE BUS

The General Purpose Interface Bus (GPIB) is an instrumentation interface for integrating instruments, calculators, and computers into systems. The bus uses sixteen signal lines to affect transfer of data and commands to as many as 15 instruments. The instruments on the bus are connected in parallel as shown in Figure 1-1. Eight of the signal lines (DIO 1 thru DIO 8) are used for the transfer of data and other messages in a byte-serial, bit-parallel form. The remaining eight lines are used for communications timing (handshake), control, and status information. Data is transmitted on the eight GPIB data lines as a series of eight-bit characters referred to as bytes. Normally, a seven-bit ASCII (American Standard Code for Information Interchange) code is used. The eighth (parity) bit is not used. Data is transferred by means of an interlocked "handshake" technique. This sequence permits asynchronous communications over a wide range of data rates. A glossary of GPIB terms with definitions of mnemonic acronyms is included in Table 1-1. The following paragraphs provide an overview description of the data, management, and handshake buses and describes how these buses interface with the sweep generator.

1-3.1 Data Bus Description

The data bus contains eight bi-directional active-low signal lines, DIO 1 thru DIO 8. One byte of information (eight bits) is transferred over the bus at a time. DIO 1 represents the least significant bit (LSB) in the byte; DIO 8 represents the most significant bit (MSB) in the byte. Each byte represents a peripheral address (either primary or secondary), a control word, or a data byte. Data bytes are formatted in ASCII code, without parity. The data bus provides the conduit for transmitting frequency and control data from the controller to the sweep generator.

1-3.2 Management Bus Description

The management bus is a group of five signal lines that are used to control the transfer of bytes over the data bus. The following paragraphs, in conjunction with the timing diagram contained in Figure 8-3, provide functional information regarding the individual management bus control lines.

a. ATN (attention). When this line is true (low), the Model 610D/Option 16 will respond to either (1) its preset listen address command, (2) the universal unlisten address command, or (3) the IEEE 488-1975-defined Group Execute Trigger command. When this line is false (high), the sweep generator, if previously addressed, will respond to normal programming.

b. IFC (interface clear). When this line is true (low), the Model 610D/Option 16 is placed into an idle or quiescent state. When in this state, the sweep generator, though inactive, retains its most recently-programmed instructions. When this line is false (high), the sweep generator, if previously addressed, will respond to normal programming.

c. REN (remote enable). When this line is true (low), the Model 610D/Option 16, if previously addressed, will respond to normal programming. When this line is false (high), the sweep generator is inhibited from responding to GPIB programming.

1-3.3 Data Byte Transfer Control (Handshake) Bus Description

Information is transferred on the data lines under control of a technique called the three-wire handshake. Detail A in Figure 8-3 illustrates a typical GPIB handshake sequence that occurs for each byte of data transmitted over the data bus. A functional description of each handshake line is provided below.

a. DAV (data valid). This control line is activated (pulled low) by a talker shortly after the talker has placed a valid data byte on the data bus. When this line is low, and if all other conditions are met (Model 610D/Option 16 has been properly addressed, ATN and REN are low, and IFC is high), the Model 610D/Option 16 will capture the data byte and complete the handshake.

b. NRFD (not ready for data). This line goes low (true) in response to the leading-edge of the DAV signal except during oscillator bandswitch. When the sweep generator RF plug-in is switching internal oscillators, the handshake sequence is delayed to allow for oscillator settling time.

c. NDAC (not data accepted). When this line goes high (false), it indicates that the data has been accepted by the Model 610D/Option 16.

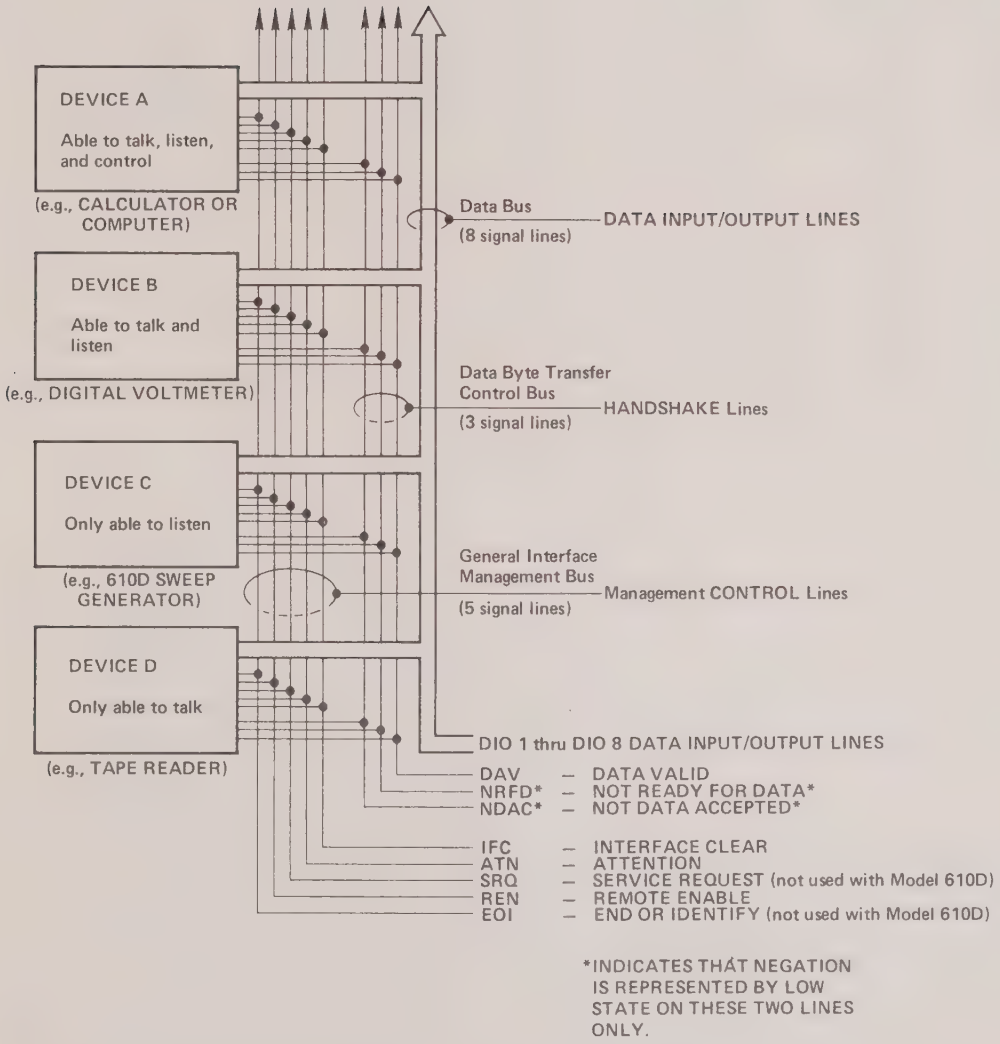

DEVICE A
Able to talk, listen, and control
(e.g., CALCULATOR OR COMPUTER)
DEVICE B
Able to talk and listen
(e.g., DIGITAL VOLTMETER)
DEVICE C
Only able to listen
(e.g., 610D SWEEP GENERATOR)
DEVICE D
Only able to talk
(e.g., TAPE READER)
Data Bus
(8 signal lines)
DATA INPUT/OUTPUT LINES
Data Byte Transfer Control Bus
(3 signal lines)
HANDSHAKE Lines
General Interface Management Bus
(5 signal lines)
Management CONTROL Lines
DIO 1 thru DIO 8 DATA INPUT/OUTPUT LINES
DAV – DATA VALID
NRFD* – NOT READY FOR DATA*
NDAC* – NOT DATA ACCEPTED*
IFC – INTERFACE CLEAR
ATN – ATTENTION
SRQ – SERVICE REQUEST (not used with Model 610D)
REN – REMOTE ENABLE
EOI – END OR IDENTIFY (not used with Model 610D)
*INDICATES THAT NEGATION IS REPRESENTED BY LOW STATE ON THESE TWO LINES ONLY.

Figure 1-1. Interface Connections and Bus Structure

Table 1-1. Glossary of Terms with Definitions of Mnemonic Acronyms

TERM OR ACRONYM	DEFINITION
Address	A seven-bit code that enables the Model 610D/ Option 16 RF Sweep Generator to listen on the data bus.
ASCII	Acronym for American Standard Code for Information Exchange. An eight-bit character code.
ATN	Attention. Mnemonic acronym for one of the management bus control lines. This control line is driven active-low (logic level 1) by the controller when peripheral devices are being assigned as listeners and talkers. Only peripheral addresses and control messages can be transferred over the data bus when ATN is active-low. After ATN goes high, only those peripheral devices which are assigned as listeners and talkers can take part in the data transfer.
Bit	Abbreviation for binary digit.
Byte	A single group of bits processed together.
Controller	Any interface bus device that is capable of setting the ATN line and addressing other bus instruments.
DAV	Data Valid. Mnemonic acronym for one of the handshake bus control lines. This line is activated by a talker shortly after the talker has placed a valid data byte on the data bus. A low (logic level 1) on this line is a signal flag for each assigned listener to capture the data byte presently on the data bus.
DIO	Data Input/Output. Mnemonic acronym for the bi-directional data transfer lines.
EOI	End or Identify. Mnemonic acronym for one of the management bus control lines. The EOI signal can be used by the talker to indicate the end of a data transfer sequency. The talker activates EOI as the last byte of data transmitted. This control line is not used by the Model 610D/ Option 16. EOI is terminated on the Option 16 A1 PC Assembly.

Table 1-1. Glossary of Terms with Definitions of Mnemonic Acronyms

TERM OR ACRONYM	DEFINITION
GPIB	General Purpose Interface Bus. Acronym used to describe the optional circuits that enable the 610D RF Sweep Generator to conform to the IEEE Standard Digital Interface for Programmable Instrumentation--IEEE Standard 488-1975.
Idle	A term used to describe the state of any device which has not been addressed. In the idle mode the Model 610D/Option 16 is inactive, but retains its previously-programmed instructions.
INC	Increment. Mnemonic term for the increment data line(s).
I/O	Input/Output.
IFC	Interface Clear. Mnemonic acronym for one of the management bus control lines. This control line is pulled active-low (logic level 1) by the controller when it wants to place all GPIB units in a predetermined quiescent state.
Listener	A device capable of receiving information transmitted over the data bus. There may be up to fourteen listeners on the bus at any one time.
MLA	My Listen Address. Mnemonic acronym for the A1 PC Assembly Address Decoder circuit output line.
NDAC	Not Data Accepted. Mnemonic acronym for one of the handshake bus control lines. This control line is held low (logic level 1) by each listener until the listener captures the data byte currently being transmitted over the data bus. When all listeners have captured the data byte, NDAC goes high (logic level 0). This line going high indicates that all listeners have accepted the data.

Table 1-1. Glossary of Terms with Definitions of Mnemonic Acronyms

TERM OR ACRONYM	DEFINITION
NRFD	Not Ready For Data. Mnemonic acronym for one of the handshake bus control lines. This control line indicates when one or more assigned listeners are not ready to receive the next data byte. Listeners are connected to the NRFD line in a logical AND configuration; consequently, this line will not go high (active state 0) until all assigned listeners are ready to receive the next data byte. When a talker recognizes that this line has gone high, it will place the next data byte on the data bus and set the DAV handshake line to its active-low (logic level 1) state.
PLA	Programmable Logic Array. Acronym for the A1 PC Assembly logic device that decodes the GPIB data bus.
REN	Remote Enable. Mnemonic acronym for one of the management bus control lines. This control line is active-low (logic level 1) whenever the system is operating under program control.
SRQ	Service Request. Mnemonic acronym for one of the management bus control lines. This control line is included so that any peripheral device on the GPIB can request the attention of a controller by setting SRQ to its active-low state. The controller responds by setting ATN true (low) and executing a serial poll to see which device is requesting service. This line is not used by the Model 610D/Option 16. SRQ is terminated on the Option 16 A1 PC Assembly.
System Controller	A GPIB instrument with all the features of of a controller plus the ability to set the IFC and REN signal lines.

Table 1-1. Glossary of Terms with Definitions of Mnemonic Acronyms

TERM OR ACRONYM	DEFINITION
Talker	A device that has the capability of placing information on the common data bus. (The interface bus system may contain several talkers; however, to eliminate confusion, the controller allows only one device to talk at any given time.)
Unaddress Command	See Unlisten Command.
Universal Command	A command that affects all interface bus devices, regardless of whether or not they have been addressed.
Unlisten Command	This command, ASCII ?, causes all devices on the bus to become unaddressed and to revert to an idle state.
UNL	Unlisten Command. Mnemonic term for unlisten command.

SECTION II
INSTALLATION

This section is not applicable to Model 610D/ Option 16. Information regarding installation is contained in the Model 610D Operation and Maintenance Manual. The electronic circuits that comprise the Option 16 assembly are installed at the factory; no further installation actions are required by the customer.

SECTION III
OPERATION

3-1. INTRODUCTION

This section includes paragraphs which describe the interface connections, addressing, operation, and unaddressing of the Model 610D/Option 16 RF Sweep Generator. This section also contains descriptions of typical test setups using the Tektronix 4051, the Hewlett-Packard 9825A, and the Commodore PET 2001 as system controllers. Information concerning performance considerations that apply when operating the sweep generator in an automatic test system are also included.

3-2. INTERFACE CONNECTIONS

3-2.1 Interface Connector

Interface between the Model 610D/Option 16 RF Sweep Generator and other devices on the bus is via a 24-wire interface cable. This interface cable is specially constructed with each end containing a connector shell with two connector faces. These double-faced connectors allow for the parallel connection of two or more cables to a single device. Figure 3-1 shows the pin assignments for the microribbon type-57 connector installed on the sweep generator rear panel. Figure 3-2 is a photograph of a WILTRON interconnect cable assembly. The WILTRON cable may be ordered by special request. Refer to Section VII for parts ordering information.

3-2.2 Cable Length Restrictions

The General Purpose Interface Bus system can accommodate up to fifteen instruments at any one time. To achieve design performance on the bus, the proper timing and voltage level relationships must be maintained. If either the cable length between separate instruments or the accumulated cable length between all instruments is too long, the data and control lines cannot be driven properly and the system may fail to perform. Cable length restrictions are as follows:

- With two instruments in a system, the cable length must not exceed four meters (12 feet).
- When more than two instruments are connected on the bus, the cable length to each instrument must not exceed two meters (6 feet) per unit.
- The total accumulative cable length between all units on the bus must not exceed 20 meters (65 feet).

3-3. ADDRESSING THE MODEL 610D/OPTION 16

Addressing the Model 610D/Option 16 RF Sweep Generator is accomplished by setting the five white ON/OFF rocker-type address switches, SW1 thru SW5 (S1 thru S5), to positions that correspond to the desired address (refer to Table 3-1 and Figure 3-3 for address switch setup instructions). The Model 610D/Option 16 may be set to respond to any listen address from 1 to 30, the only restriction being that no two GPIB devices share the same address code. The address switch rocker arms are preset at the factory for a listen address of 5.

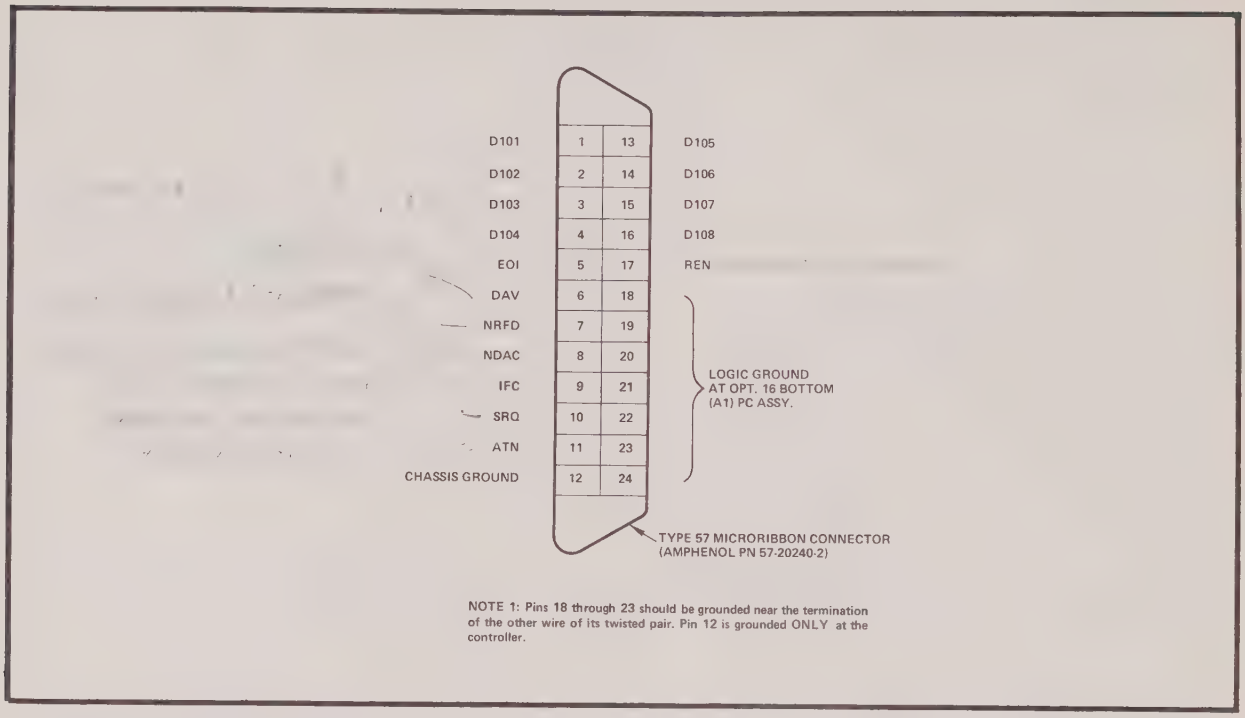
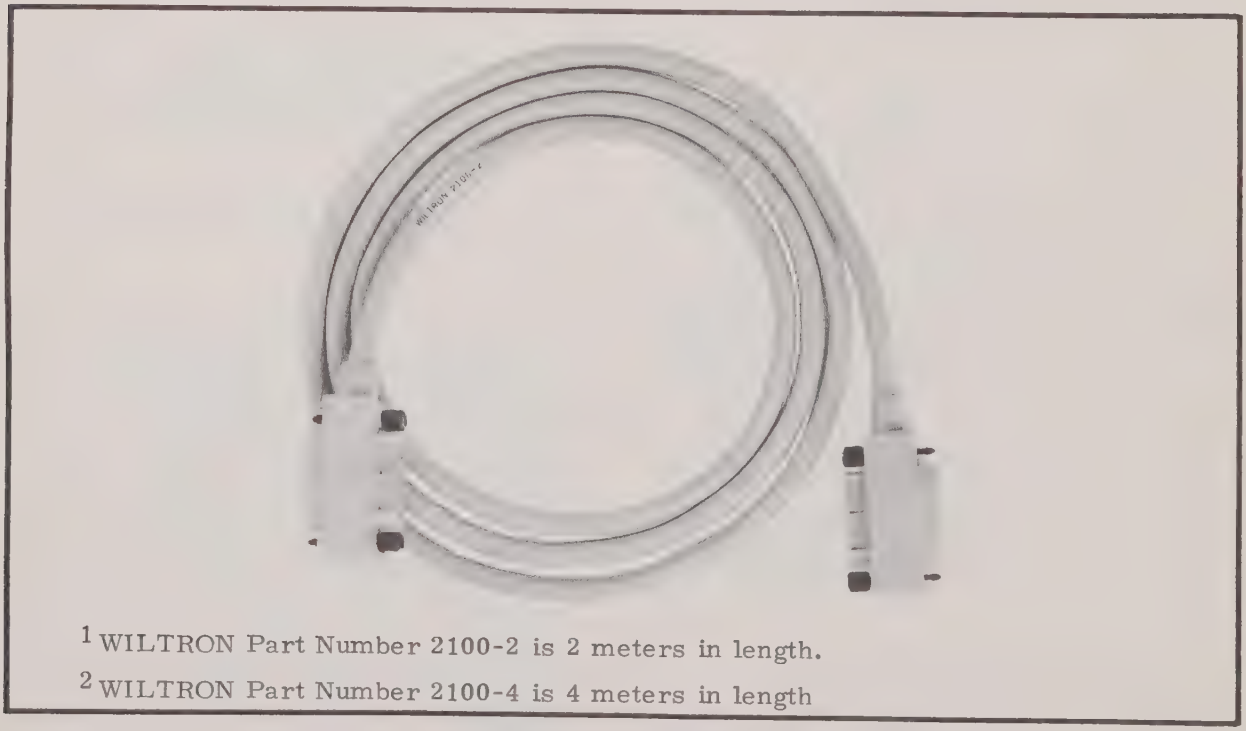

D101 1 13 D105
D102 2 14 D106
D103 3 15 D107
D104 4 16 D108
EOI 5 17 REN
DAV 6 18
NRFD 7 19
NDAC 8 20
IFC 9 21
SRQ 10 22
ATN 11 23
CHASSIS GROUND 12 24
LOGIC GROUND AT OPT. 16 BOTTOM (A1) PC ASSY.
TYPE 57 MICRORIBBON CONNECTOR (AMPHENOL PN 57-20240-2)
NOTE 1: Pins 18 through 23 should be grounded near the termination of the other wire of its twisted pair. Pin 12 is grounded ONLY at the controller.

Figure 3-1. Model 610D/Option 16 Rear Panel Interface Connector



[1] WILTRON Part Number 2100-2 is 2 meters in length.

[2] WILTRON Part Number 2100-4 is 4 meters in length

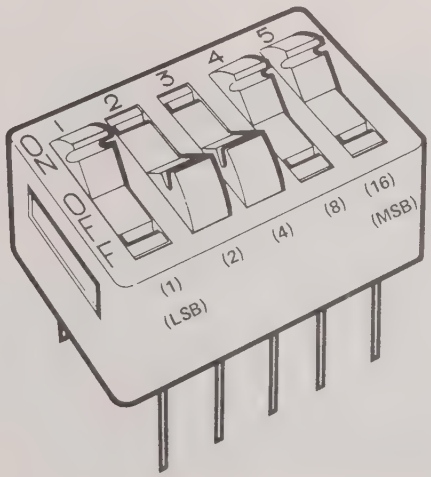
Figure 3-2. GPIB System Interconnect Cable, WILTRON Part Numbers 2100-2, 2100-4

Table 3-1. Available Address Codes

Decimal Address	ASCII Character	(MSB) SW 5	SW 4	SW 3	SW 2	(LSB) SW 1
1	!	0	0	0	0	1
2	"	0	0	0	1	0
3	#	0	0	0	1	1
4	$	0	0	1	0	0
5	%	0	0	1	0	1
6	&	0	0	1	1	0
7	'	0	0	1	1	1
8	(	0	1	0	0	0
9	)	0	1	0	0	1
10	*	0	1	0	1	0
11	+	0	1	0	1	1
12	,	0	1	1	0	0
13	-	0	1	1	0	1
14	.	0	1	1	1	0
15	/	0	1	1	1	1
16	0	1	0	0	0	0
17	1	1	0	0	0	1
18	2	1	0	0	1	0
19	3	1	0	0	1	1
20	4	1	0	1	0	0
21	5	1	0	1	0	1
22	6	1	0	1	1	0
23	7	1	0	1	1	1
24	8	1	1	0	0	0
25	9	1	1	0	0	1
26	:	1	1	0	1	0
27	;	1	1	0	1	1
28	<	1	1	1	0	0
29	=	1	1	1	0	1
30	>	1	1	1	1	0

Switch ON = 0

Switch OFF = 1



NOTE: The parenthesized number under each switch represents the binary weight of the switch when it is depressed to the OFF position. The ON position of the switch represents a binary 0. An example of a typical switch setup is as follows: Listen Address = 25--S1-OFF, S2-ON, S3-ON, S4-OFF, S5-OFF.

Figure 3-3. Address Switches S1 thru S5 (SW1 thru SW5)

3-4. OPERATING THE MODEL 610D/ OPTION 16

Computer-controlled operation of the Model 610D/Option 16 RF Sweep Generator is accomplished using a system of ASCII (American Standard Code for Information Interchange) coded control and frequency data instructions. The signals and codes that convey these instructions are discussed in paragraphs 3-4.2 thru 3-4.6. Operational programming for the sweep generator is generally accomplished through programming statements being input to the GPIB System Controller. There are, however, several Model 610D/Option 16 controls, switches, and potentiometers that must be set and/or adjusted to permit the sweep generator to respond properly to computer-control. The controls referred to are front panel controls. Front panel control settings are described in paragraph 3-4.1. The switches and potentiometers referred to are the address switches, described in paragraph 3-3, and the range potentiometers, described in paragraph 3-4.3.

3-4.1 Operation of Front Panel Controls

For proper programming responses, the Model 610D/Option 16 RF Sweep Generator front panel sweep mode control must be positioned as specified in Figure 3-4.

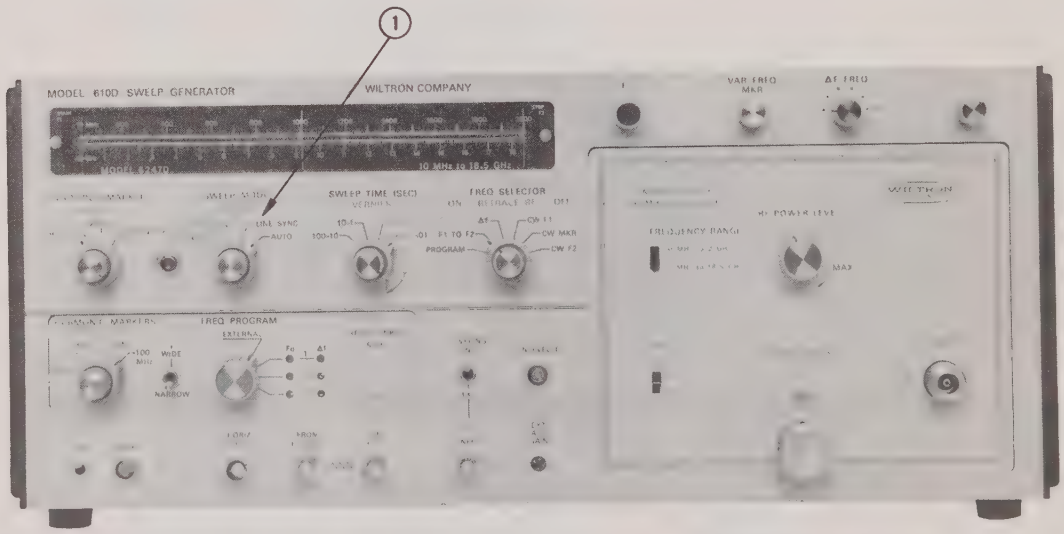
3-4.2 Mode Operation

The Model 610D/Option 16 RF Sweep Generator operates in any one of four controller-selected modes. These modes and the ASCII characters that initiate their operation are listed below.

a. Mode 0. In this mode, the sweep generator responds only to local (front and rear panel) control. The sweep generator is placed in this mode as follows:

(1) Each time power is applied the sweep generator comes up in mode 0.

(2) The controller sends MØ over the bus.



(1) SWEEP MODE - Control must be in MANUAL when programmed in modes 1 or 2. Control must be in TRIG when programmed in mode 3.

Figure 3-4. Model 610D/Option 16 Front Panel Controls

b. Mode 1. In this mode, the sweep generator may be programmed to respond to frequency tuning either: (1) across the entire frequency range of the RF plug-in or (2) across a range of frequencies determined by the settings of the range potentiometers. The sweep generator is placed in this mode when the controller sends M1 over the bus.

c. Mode 2. In this mode, the range over which the sweep generator tunes its frequency is controlled by front panel frequency controls (FREQ SELECTOR, F1, F2, VAR FREQ MKR, and Δ FREQ). The frequency range is determined by a combination of the FREQ SELECTOR control and either the F1 and F2 controls or the VAR FREQ MKR and Δ FREQ controls; individual frequency points within this selected range are determined by the controller. The sweep generator is placed in this mode of operation when the controller sends M2 over the bus.

d. Mode 3. In this mode, the sweep generator frequency tuning sweep is triggered by the controller. Also, the in/out status of the CW filter is determined by the controller; all other sweep generator functions are determined by front panel controls. The sweep generator is placed in this mode of operation when the controller sends M3 over the bus.

3-4.3 Range Operation

The Model 610D/Option 16 RF Sweep Generator contains a range selection circuit that provides for the programming of any one of four different frequency ranges. This circuitry consists of four potentiometer-pairs that are used to establish upper and lower frequency limits. These potentiometer-pairs are active only during Mode 1 operation. The sweep ranges and the ASCII characters that initiate them are defined below.

a. Range Ø. This range, initiated by ASCII characters R and Ø, provides for up to 10,000 points of frequency tuning across the full range of the installed RF plug-in.

b. Range 1. This range provides for up to 10,000 points of frequency tuning between the frequency limits set by potentiometer-pairs R17 (F1) and R18 (F2). The sweep generator is placed in this mode when the controller sends R1 over the bus.

c. Range 2. This range provides for up to 10,000 points of frequency tuning between the frequency limits set by potentiometer-pairs R19 (F1) and R20 (F2). The sweep generator is placed in this mode when the controller sends R2 over the bus.

d. Range 3. This range provides for up to 10,000 points of frequency tuning between the frequency limits set by potentiometer-pairs R21 (F1) and R22 (F2). The sweep generator is placed in this mode when the controller sends R3 over the bus.

e. Range 4. This range provides for up to 10,000 points of frequency tuning between the frequency limits set by potentiometer-pairs R23 (F1) and R24 (F2). The sweep generator is placed in this mode when the controller sends R4 over the bus.

3-4.4 CW Filter Operation

A low-pass filter (CW filter) is installed in the sweep generator mainframe to filter inherent noise spikes from the oscillator input voltage lines. If not filtered, these noise spikes may cause the oscillator output frequency to become frequency modulated. However, whereas the filtering of the oscillator control voltages will minimize residual frequency modulation, the presence of this filter in the circuit will inhibit rapid changes to the oscillator output frequency. Filter control (the ability to switch the filter in and out of the circuit) is provided in two ways: (1) In mode 0 (MØ), the filter is controlled by the rear panel FM-NORM switch. (2) In mode 1 (M1), mode 2 (M2),

and mode 3 (M3) the filter is controlled as follows: when the filter is to be switched into the circuit, the controller sends F and I over the bus; when the filter is to be switched out of the circuit, the controller sends F and O over the bus.

3-4.5 Frequency Operation (General)

The Model 610D/Option 16 RF Sweep Generator output frequency is generated by a voltage-controlled oscillator, a type of frequency source that lends itself to computerized programming. To tune the Model 610D/Option 16 to a particular frequency, a tuning system has been devised that uses a sequence of numbers from 0 to 9999. The mathematical formulas used to calculate the number (N) that corresponds to a particular frequency and, conversely, the frequency that corresponds to a particular value of N, are shown below. The two numbers (9755.9 and 109.73) used in these formulas are offset numbers whose values have been chosen to be compatible with the sweep generator frequency tuning. The sweep generator is tuned to provide a margin-of-error on each end of the frequency band. The margin is approximately 1% of full-band, and it is used to compensate for minor variations in frequency band edges due to temperature. This error margin insures coverage over the entire range of RF plug-in frequencies.

In the two formulas given below, the lower (F_L) and the upper (F_H) frequency limits depend upon the operational mode and range programmed (for modes 1 and 2 only; modes 0 and 3 depend upon front panel controls). Frequency limit values are determined as follows:

a. Mode 1. In this mode, the frequency limits depend upon the range that has been programmed; they are determined as follows:

(1) In range 0 (RØ), F_L and F_H are the lower and the upper frequency limits of the RF plug-in.

(2) In ranges 1 thru 4 (R1 thru R4), F_L and F_H depend upon the settings of RNG 1 thru RNG 4, F1 and F2 potentiometers. These potentiometers must be adjusted so that the frequency starts at F1 and sweeps up in frequency to F2. Consequently, the frequency value of F1 must be equal to or less than that of F2 (F1 ≤ F2).

b. Mode 2. In this mode, F_L and F_H depend upon the positioning of the following front panel controls:

(1) FREQ SELECTOR (F1 TO F2) and the F1 and F2 controls.

(2) FREQ SELECTOR (Δ FREQ) and the VAR FREQ MKR and Δ FREQ controls.

(3) If Option 4 is installed, FREQ SELECTOR (PROGRAM) and the FREQ PROGRAM-EXTERNAL control.

Formulas for determining either the number (N) from a given frequency (F_O) or a frequency from a known value of N are:

(1) Calculating N when F_O is given:

$$N = \left(\frac{F_O - F_L}{F_H - F_L} \right) 9780.1 + 109.4$$

(2) Calculating F_O when N is known:

$$F_O = \frac{(N - 109.4)\ (F_H - F_L) + F_L\ 9780.1}{9780.1}$$

where N = The frequency point number. After calculation, this number must be rounded to either the next lower or next higher integer (whole number). Decimal points are not recognized by the Option 16 circuitry (refer to paragraph 3-4.7).

F_O = Desired frequency

F_L = Lower frequency limit

F_H = Upper frequency limit

3-4.6 Frequency Operation (Incremental)

To simplify frequency updating, a method of incrementing N (refer to paragraph 3-4.5) has been included in the sweep generator Option 16 circuitry. This incremental frequency programming is accomplished by sending only one ASCII character over the bus, instead of the three to six characters required with standard programming. When sending incremental data over the bus, the prefix and suffix characters (V and E) normally used in frequency programming are not used. Also, when a rapid or small (1-unit) change in frequency is desired, two or more of these characters may be "strung" together following one Address Listen command (refer to paragraph 3-4.7). Be advised, however, that when programming for rapid changes in frequency over a large frequency range, oscillator settling time (paragraph 3-8.1) may need to be considered.

The increment characters (ASCII) and the decade-digit of N that each one increments are as follows:

- O increments the decade-digit 10^0 (increases N by 1 unit).
- T increments the decade-digit 10^1 (increases N by 10 units).
- H increments the decade-digit 10^2 (increases N by 100 units).
- K increments the decade-digit 10^3 (increases N by 1000 units).

3-4.7 Frequency Programming Commands (Characteristics and Examples)

a. Characteristics. To cause the sweep generator to respond to a specific frequency, the number (N) that corresponds to that frequency is placed on the data bus, preceeded by the ASCII character V (voltage). This number may contain from one to four digits, depending upon the desired frequency. The ASCII character E (end) must follow N's last digit. To avoid frequency errors, certain rules accompany the composition of N. These rules are as follows:

(1) Leading zeros are suppressed at the sweep generator, i.e., V0003E is the same as V3E (3rd frequency point).

(2) The sweep generator recognizes only the first four digits of a frequency data transmission, i.e., V12345E will be read as V1234E (1234th frequency point).

(3) The sweep generator does not recognize either alpha or non-numeric characters (for the Model 610D/ Option 16, the computer characters +, -, E, ., space, etc. are classified as non-numerics); i.e., V21C3E will be read as V213E (213th frequency point), V-50E will be read as V50E (50th frequency point).

(4) The sweep generator recognizes only integers (whole numbers) (decimal points are ignored); i.e., V40.5E will be read as V405E (405th frequency point).

b. Examples. Typical programming commands are illustrated in Table 3-2 and Table 3-3.

3-4.8 Summary of Program Codes

A summary of available program codes for mode 1, mode 2, mode 3, and mode 4 are contained in Tables 3-4, 3-5, 3-6, and 3-7, respectively.

Table 3-2. Programming Examples (Single Frequency)

The Model 6237D RF Plug-In (2.0 to 18.5 GHz) is installed and a frequency of 4.0 GHz is desired. By using the formula shown below, the number (N) is found to be 1295.

$$N = \text{INT}\left[\left(\frac{F_O - F_L}{F_H - F_L}\right) \quad 9780.1 + 109.4\right]$$

where INT = Integer Number

F_O = Desired Frequency (4.0 GHz)

F_L = Lower Frequency Limit (2.0 GHz)

F_H = Upper Frequency Limit (18.5 GHz)

Command: M1 RØ FO V1295E

- V1295E — Frequency Code = 4.0 GHz (paragraph 3-4.7)
- FO — CW Filter Out (paragraph 3-4.4)
- RØ — Range Zero (paragraph 3-4.3)
- M1 — Mode 1 (paragraph 3-4.2)

Table 3-3. Programming Commands (Swept-Frequency)

It is desired to sweep the entire frequency range of the Model 6237D (2.0 to 18.5 GHz) RF Plug-In in ten steps. Three methods are available for accomplishing this sweep, as described below:

(1) Standard Programming:

Command #1: M1RØFOV1Ø9E (Settling Time) (See Note)

Command #2: V11Ø9E (Settling Time)

Command #3 thru Command #9: Same format as Command #2; number increases by 1ØØØ with each Command.

Command #10: V989ØE

(2) Incremental Frequency Programming with Settling Time Allowed between Increments:

Command #1: M1RØFOV1Ø9E (Settling Time) (See Note)

Command #2 thru Command #9: K (Settling Time)

Command #10: K (Sweep returns to lower limit)

(3) Incremental Frequency Programming with No Settling Time Allowed between Increments:

Command: MIRØFOV1Ø9EKKKKKKKKKK (See Note)

NOTE

If precise frequency definition is important, a specified time (settling time, see paragraph 3-8.1) should be allowed between each change in frequency points. If, however, precise frequency is unimportant and only a sweep ramp is desired, settling time need not be considered.

Table 3-4. Summary of Mode 0 Program Codes

PROGRAM	ASCII CHARACTER	NOTES
Entry Into Mode 0	MØ	No program codes are available. Each time power is applied, the sweep generator will come up in Mode 0 (local mode), regardless of front panel control settings.

Table 3-5. Summary of Mode 1 Program Codes

PROGRAM	ASCII CHARACTER	NOTES
Entry Into Mode 1	M1	Front panel SWEEP MODE control must be in MANUAL.
RANGE DATA:		
Range 0	RØ	Only one of these ranges may be selected at any one time. Refer to paragraph 3-4.3.
Range 1	R1	
Range 2	R2	
Range 3	R3	
Range 4	R4	
CW FILTER DATA:		
Filter In	FI	Refer to paragraph 3-4.4.
Filter Out	FO	
FREQUENCY DATA:		
Maximum 4-digit number as determined by formula	V - - - - E	The frequency number may go from VØE to V9999E. Refer to paragraph 3-4.5.
INCREMENT FREQUENCY:		
Frequency may be incremented by units, tens, hundreds, and thousands.	0 - units T - tens H - hundreds K - thousands	Refer to paragraph 3-4.6.

Table 3-6. Summary of Mode 2 Program Codes

PROGRAM	ASCII CHARACTER	NOTES
Entry Into Mode 2	M2	Front panel SWEEP MODE control must be in MANUAL. Upper and lower sweep limits are defined by front panel frequency controls, i.e., a combination of either the FREQ SELECTOR plus F1 and F2 or the FREQ SELECTOR plus VAR FREQ MKR and Δ FREQ.
RANGE DATA: Determined by F1/F2 or VAR FREQ MKR/ΔFREQ controls.	None	Refer to paragraph 3-4.2.
CW FILTER DATA: Filter In Filter Out	 FI FO	Refer to paragraph 3-4.4.
FREQUENCY DATA: Maximum 4-digit number as determined by formula.	V - - - - E	The frequency number may go from VØE to V9999E. Refer to paragraph 3-4.5.
INCREMENT FREQUENCY: Frequency may be incremented by units, tens, hundreds, and thousands.	O - units T - tens H - hundreds K - thousands	Refer to paragraph 3-4.6.

Table 3-7. Summary of Mode 3 Program Codes

PROGRAM	ASCII CHARACTER	NOTES
Entry Into Mode 3	M3	Front panel SWEEP MODE control must be in TRIG. Sweep generator responds to manual operation of all other front panel controls.
TRIGGERING DATA: Model 610D Only Trigger Group Execute Trigger	 T BS (Backspace)	 Refer to paragraph 3-4.2
CW FILTER: Filter In Filter Out	 FI FO	 Refer to paragraph 3-4.4.

3-5. UNADDRESSING THE MODEL 610D/OPTION 16

Unaddressing the Model 610D/Option 16 RF Sweep Generator means taking the sweep generator off-line and placing it in an idle state. The sweep generator may be unaddressed in any of the following three ways:

- a controller sends the universal unlisten address (UNL) command, ASCII character ?, over the data bus.

- the system controller places the Interface Clear (IFC) management bus line to its active-low (logic level 1) state. (The active state of this line clears all bus instruments and causes them to revert to their idle state.)

- each time power is applied the Power-On Reset Generator (PON) circuit clears listen flip-flop U17 (refer to paragraph 4-3).

3-6. ADJUSTMENT OF RANGE POTENTIOMETERS

As described in paragraph 3-4.3, mode 1 operation provides for the establishment of up to four separate, distinct, swept-frequency ranges. Four sets of potentiometers (R17-R18, R19-R20, R21-R22, R23-R24) installed on the top (A2) PC assembly are used for establishing these sweep limits. The procedure for setting up the range potentiometers is provided in Table 3-8, RNG 1 thru RNG 4, F1 and F2 Frequency Adjustments. This procedure is arranged so that it will be compatible with any of the GPIB system controllers commonly in use. In the procedure, the ASCII command given for each procedural step is the command that the Option 16 circuits need to "see." In order for these commands to be placed on the bus, however, they will have to be incorporated into a programming statement that the System Controller can use. For example, a BASIC (computer language) programming statement, as used by the Tektronix 4051, might look like the following: PRI@5: "M1RØFIV11ØE" (RETURN) (Sweep Generator address set to 5.)

Table 3-8. RNG 1 thru RNG 4, F1 and F2 Frequency Adjustments (Page 1 of 2)

STEP	ASCII COMMAND	PROCEDURE
		Preliminary Procedure
1.	N/A	Configure the Interface Bus with a system controller and a Model 610D/Option 16 RF Sweep Generator. Obtain a frequency counter capable of measuring the desired frequencies.
2.	N/A	Connect a suitable coaxial cable between the RF OUTPUT on the Model 610D RF Plug-In and the frequency input connector on the frequency counter.
3.	N/A	Turn on bus instruments and frequency counter; allow for the required equipment warm-up.
4.	N/A	Position frequency counter controls to obtain the necessary frequency readout.

Table 3-8. RNG 1 Thru RNG 4, F1 and F2 Frequency Adjustments (Page 2 of 2)

STEP	ASCII COMMAND	PROCEDURE
		Adjustment Procedure
5.	M1 R1 FI V1Ø9E	Adjust RNG 1-F1 (R17) for the user-defined lower frequency limit.
6.	V989ØE	Adjust RNG 1-F2 (R18) for the user-defined upper frequency limit.
7.	R2 V1Ø9E	Adjust RNG 2-F1 (R19) for the user-defined lower frequency limit.
8.	V989ØE	Adjust RNG 2-F2 (R20) for the user-defined upper frequency limit.
9.	R3 V1Ø9E	Adjust RNG 3-F1 (R21) for the user-defined lower frequency limit.
10.	V989ØE	Adjust RNG 3-F2 (R22) for the user-defined upper frequency limit.
11.	R4 V1Ø9E	Adjust RNG 4-F1 (R23) for the user-defined lower frequency limit.
12.	V989ØE	Adjust RNG 4-F2 (R24) for the user-defined upper frequency limit.

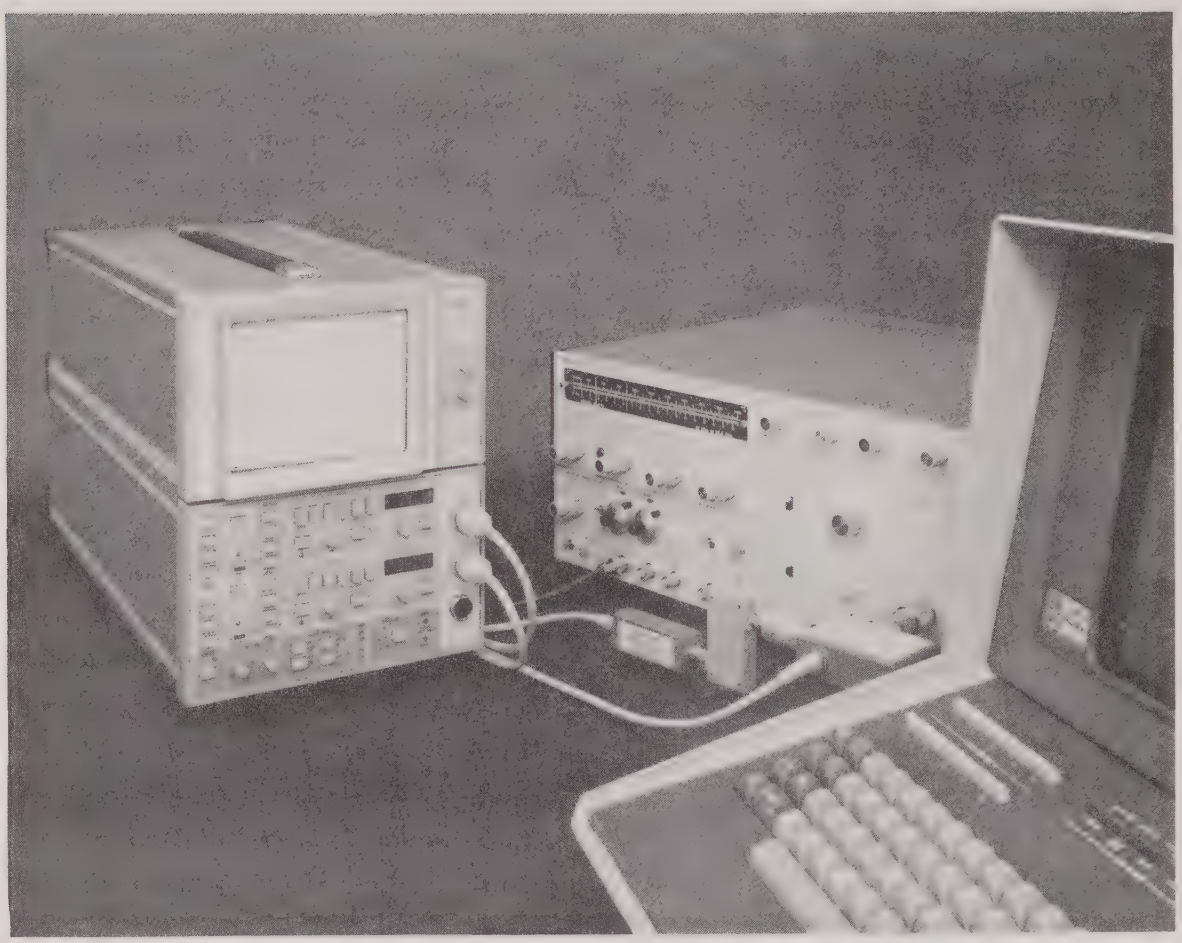


Figure 3-5. Typical GPIB, showing the Model 610D/Option 16 RF Sweep Generator, the Tektronix 4051 Graphic System, and the Model 560 Scalar Network Analyzer

3-7. PROGRAMMING THE SYSTEM CONTROLLER

The Model 610D/Option 16 RF Sweep Generator is capable of being programmed by several different computer types. The three models of computer/calculator system most commonly used as GPIB System Controllers are: Tektronix 4051 Graphic System, Hewlett-Packard 9825A Programmable Calculator System, and Commodore PET 2001 Series Personal Computer System. Even though these three computers are different in design, overall capability, and, in the case of Hewlett-Packard, programming language (Tektronix and Commodore use BASIC; Hewlett-Packard uses HPL), they all have certain similarities. All of these computers are capable of communicating with the "outside world", using a system of ASCII characters.

Programming these three computers to communicate with the Model 610D/Option 16 is discussed in the following paragraphs; sample programs are given in Figures 3-6, 3-7, and 3-8. In all of the examples given, the Model 610D/Option 16 is assumed to be configured for operation at address 5. The address 5 statements as shown for the Tektronix, Hewlett-Packard, and Commodore systems are PRI@5, wrt 705, and PRINT#5, respectively.

3-7.1 Programming with the Tektronix 4051

Programming the Tektronix 4051 Graphic System to communicate with the Model 610D/Option 16 RF Sweep Generator can be accomplished in two different ways: individual keyboard commands or computer program. Individual keyboard commands are illustrated below; a simple computer program is shown in Figure 3-6.

Individual Keyboard Commands (Examples):

PRI@5: "M1" (Depress RETURN key) - This command places the sweep generator in mode 1.

PRI@5: "F1" (Depress RETURN key) - This command activates the CW filter.

PRI@5: "M1R1V5ØØØE" (Depress RETURN key) - This command places the sweep generator in mode 1, range 1 operation, and sets the output frequency to approximately the middle of Range 1--RNG 1 as defined by potentiometers R17-R18, see paragraph 3-6.

PROBLEM: Using a Model 610D/Option 16 with Model 6237D RF Plug-In (2 to 18.5 GHz), generate a sequence of 10 equally-spaced frequencies between 4.0 and 7.5 GHz.

PROGRAM:

```
1ØØ F1 = 2ØØØ
11Ø F2 = 185ØØ      (To provide flexibility, these two variables may be written as INPUT statements.)
12Ø PRI @ 5: "M1RØ"
13Ø FOR N = 1 TO 1Ø
14Ø F = 4000 + (75ØØ-4ØØØ)/9 * (N-1)
15Ø V = (F-F1) * 978Ø.1/(F2-F1) + 1Ø9.4
16Ø V = INT(V)       (This operator insures that V is an integer number.)
17Ø PRI @ 5: "V";V;"E"
18Ø FOR L = 1 TO 1Ø
190 NEXT L           (These two statements provide oscillator settling time.)
2ØØ NEXT N
21Ø END
```

Figure 3-6. Sample Computer Program in BASIC (Tek 4051)

3-7.2 Programming with the Hewlett-Packard 9825A

Programming the Hewlett-Packard 9825A to communicate with the Model 610D/Option 16, like the Tektronix 4051 previously described, can be accomplished in two ways. The Model 610D/Option 16 will respond to individual keyboard commands or it will respond to a computer program. Individual keyboard commands are illustrated below; a simple computer program is shown in Figure 3-7.

Individual Keyboard Commands (Examples):

wrt 705, "M1" (Depress RETURN key) -	This command places the sweep generator in mode 1.
wrt 705, "FI" (Depress RETURN key) -	This command activates the CW filter.
wrt 705, "M1R1V5ØØØE" (Depress RETURN key) -	This command places the sweep generator in mode 1, range 1 operation, and sets the output frequency to approximately the middle of range 1 (RNG 1 as defined by potentiometers R17 - R18, see paragraph 3-6).

```
PROBLEM: Using a Model 610D/Option 16 with Model 6237D RF Plug-In
         (2 to 18.5 GHz), generate a sequence of 10 equally-spaced
         frequencies between 4.0 and 7.5 GHz.

PROGRAM:

 Ø  2ØØØ⟶r1
 1  185ØØ⟶r2
 2  4ØØØ⟶T
 3  (75ØØ-4ØØØ)/9⟶I
 4  Ø⟶N
 5  "AGAIN":  T + N * I⟶F
 6  (F-r1) * 978Ø.1/(r2-r1) + 1Ø9.4⟶V
 7  int V⟶V                    (This operator insures that V is an integer number.)
 8  "V" & str (V) & "E"⟶V$
 9  wrt 7Ø5, "M1RØ", V$
10  wait 5Ø                    (This statement provides oscillator settling time.)
11  N + 1⟶N
12  if N > 9; gto "LAST"
13  gto "AGAIN"
14  "LAST":  end
```

Figure 3-7. Sample Computer Program in HPL (HP 9825A)

3-7.3 Programming with the Commodore PET 2001 Series

Programming the PET 2001 Series computer to communicate with the Model 610D/ Option 16, like the Tektronix and Hewlett-Packard controllers previously described, can also be accomplished in two ways. The Model 610D/Option 16 will respond to individual keyboard commands or it will respond to a computer program. Individual keyboard commands are illustrated below; a simple computer program is shown in Figure 3-8.

Individual Keyboard Commands (Examples):

OPEN 5, 5 (Depress RETURN key) PRINT#5, "M1" (Depress RETURN key) CLOSE 5 (Depress RETURN key)	This command places the sweep generator in mode 1.
OPEN 5, 5 (Depress RETURN key) PRINT #5, "FI" (Depress RETURN key) CLOSE 5 (Depress RETURN key)	This command activates the CW filter.
OPEN 5, 5 (Depress RETURN key) PRINT#5, "M1R1V5ØØØE" (Depress RETURN key) CLOSE 5 (Depress RETURN key	This command places the sweep generator in mode 1, range 1 operation, and sets the output frequency to approximately the middle of range 1 (RNG 1 as defined by potentiometers R17 - R18, see paragraph 3-6).

PROBLEM: Using a Model 610D/Option 16 with Model 6237D RF Plug-In (2 to 18.5 GHz), generate a sequence of 10 equally-spaced frequencies between 4.0 and 7.5 GHz.

PROGRAM:

```
1ØØ  F1 = 2ØØØ
11Ø  F2 = 185ØØ      (To provide flexibility, these two variables could be written as INPUT statements.)
12Ø  OPEN 5, 5
13Ø  PRINT #5, "M1RØ"
14Ø  FOR N = 1 TO 1Ø
15Ø  F = 4ØØØ + (75ØØ-4ØØØ)/9 * (N-1)
16Ø  V = (F-F1) * 978Ø.1/(F2-F1) + 1Ø9.4
17Ø  V = INT(V)        (This operator insures that V is an integer number.)
18Ø  PRINT #5, "V";V;"E"
19Ø  FOR L = 1 TO 1Ø      (These two statements provide oscillator settling time.)
2ØØ  NEXT L
21Ø  NEXT N
22Ø  CLOSE 5
23Ø  END
```

Figure 3-8. Sample Computer Program in BASIC (PET 2001)

3-8. PERFORMANCE CONSIDERATIONS

3-8.1 Performance

Two factors inherent in the use of RF measurement devices need to be considered when using the Model 610D/Option 16 RF Sweep Generator. These two factors, settling time and frequency accuracy, are described below.

a. Settling Time. Settling time is defined as the time required for the sweep generator output frequency to reach its final value after a step-change in input voltage. Settling time is difficult to quantify because it depends on a number of factors, such as:

- frequency range of the RF plug-in.
- magnitude of the frequency step being made, i.e., the number of voltage points between the old and new frequency settings.
- whether oscillator bandswitching is required. (Bandswitching means the switching from one oscillator to another within the RF plug-in. Many of the RF plug-ins require the use of more than one oscillator to cover their assigned frequency ranges.)
- frequency accuracy, i.e., how close to the desired frequency is acceptable.

NOTE

The sweep generator's internal CW filter has a significant effect on settling time. If settling times of less than fifty milliseconds are required, the CW filter should be switched out.

b. Frequency Accuracy. Most of the available RF plug-ins use a YIG element to control a transistor or Gunn-diode oscillator. Even though this type of frequency source is ordinarily quite linear, there are several limiting factors. Three of these factors -- absolute accuracy, linearity, and hysteresis -- are specified below.

Absolute Accuracy: This is determined by calibration of the instrument. Typical accuracies are from ± 0.3% to 1% of plug-in bandwidth.

Linearity: Specification better than ± 0.1% are typical.

Hysteresis: 0.1% is typical.

NOTE

Hysteresis can usually be minimized by programming the sweep so that the frequency is approached from the same direction each time.

3-8.2 Improving Frequency Accuracy

Two methods of improving the frequency accuracy of the Model 610D/Option 16 RF Sweep Generator are presently available. Both of these methods require the use of a microwave frequency counter; one method uses the frequency counter in an open-loop configuration while the second uses the frequency counter in a closed-loop configuration. The closed-loop method provides the greatest degree of accuracy, but requires a particular type of frequency counter -- an EIP Model 371 Source Locking Microwave Counter. These two methods are described below.

a. Method 1. This method (Figure 3-9) requires that a microwave frequency counter

be installed on the GPIB to count the output frequency of the sweep generator. The sweep generator output-frequency count is then fed back to the controller who uses it to establish iterative software control of the sweep generator. Through the use of this iterative software control, the sweep generator output frequency may be held to an accuracy of several hundred kilohertz. However, because of the open-loop type of control this method employs, if the output frequency is not frequently corrected the sweep generator may be subject to a slight drifting in frequency over the long term.

b. Method 2. This method requires the use of the EIP Model 371 Source Locking Microwave Counter in a closed-loop configuration (see Figure 3-10). This method, a closed-loop setup in which the output frequency of the sweep generator is locked to the accuracy of the frequency counter's time base, also provides long-term frequency stability. As shown in the figure, a test cable is connected between the Ø LOCK OUTPUT connector on the frequency counter rear panel and the EXT FM INPUT connector. To improve response time, the FM/NORM switch on the sweep generator rear panel should be in the FM position and the filter out command, FO, sent over the bus.

NOTE

Slightly better signal quality can be realized by using an RF plug-in that incorporates the Option 28 phase lock capability. This option provides a wider bandwidth amplifier and permits operation with the FM/NORM switch in the NORM position.

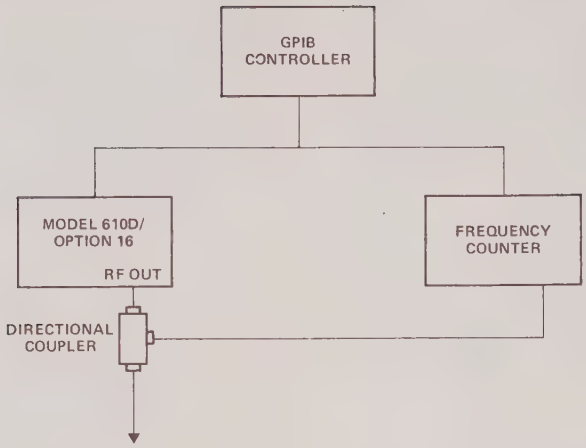


Figure 3-9. Frequency Counter Used in an Open-Loop Configuration

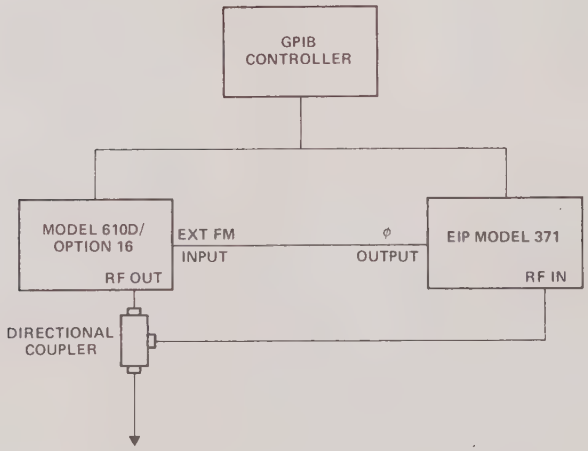


Figure 3-10. Frequency Counter in a Closed-Loop Configuration

SECTION IV
FUNCTIONAL DESCRIPTION

4-1. INTRODUCTION

This section provides a functional description of the Model 610D/Option 16 RF Sweep Generator GPIB circuitry. The Option 16 circuits consist of two printed circuit (PC) assemblies, a chassis-mounted voltage regulator (VRI), and their associated wiring and connectors. An over-all description of these circuits is provided in paragraph 4-2. Paragraph 4-2 describes the interface between: (1) the two PC assemblies and (2) the top PC assembly and the sweep generator mainframe and RF plug-in assemblies. The individual PC assembly circuit descriptions are provided in paragraphs 4-3 and 4-4.

4-2. OVERALL CIRCUIT DESCRIPTION

The Model 610D RF Sweep Generator Option 16 circuits are contained on two printed circuit (PC) assemblies. The bottom (A1) PC assembly (610D-L-6100-3) contains the digital control circuits, and the top (A2) PC assembly (610D-L-6101-3) contains the digital-to-analog conversion and operational-mode switching circuits. A functional block diagram that illustrates the relationship between the two PC assemblies is provided in Figure 4-1. As shown in this figure, the interface bus is applied to the A1 PC Assembly. The A1 PC Assembly decodes this data and, as applicable, converts the data into operational-mode, range, increment, CW filter, and trigger control voltages. Also, through a parallel transfer, the four least-significant bits are removed from the data bus and routed directly to the A1 output pins. These four bits contain numerical frequency-point data arranged in a binary-coded-decimal (BCD) format.

The control voltages, as specified above, and the BCD data-bus bits are applied to the top (A2) PC assembly.

The top (A2) PC assembly contains the digital-to-analog conversion circuits and, via an arrangement of solid-state switches, provides output control of the sweep generator. As shown in Figure 4-1, the RF plug-in oscillator tuning voltages may come from either of two sources: the sweep generator mainframe or the Option 16 digital-to-analog converter (DAC). If the A1 Assembly has decoded mode 0 (MØ) or mode 3 (M3) from the GPIB data bus, the oscillator tuning voltage is provided by the sweep generator mainframe. If mode 2 (M2) has been decoded, the tuning voltage is supplied by the DAC, via the Frequency Instruction Assembly; if mode 1 (M1) has been decoded, the tuning voltage is supplied by the DAC, via the Range Selector circuit.

The other A2 Assembly control lines are routed as shown (Figure 4-1). The TRIG control line provides a positive trigger pulse that is applied to the sweep generator mainframe during mode 3 operation. The REM FIL control line provides a voltage that controls the in/out status of the CW filter during mode 1, mode 2, and mode 3 operation; filter control during mode 0 operation is provided by the rear panel FM/NORM switch. The TTL DWL control line is an input line to the A1 Assembly. The voltage on this line, oscillator dwell voltage, is provided by the RF plug-in. This oscillator dwell voltage is generated by the RF plug-in when the switching of internal oscillators occurs. Dwell voltage is applied to the A2 PC Assembly, translated to a TTL logic level, and subsequently applied to the A1 PC Assembly.

4-3. FUNCTIONAL DESCRIPTION, BOTTOM PC ASSEMBLY (A1)

The A1 PC Assembly contains the digital logic circuits that enable the sweep generator to respond to interface bus control. This board is composed of GPIB management, data retrieval, and handshake control circuits. A functional block diagram of this circuit assembly is provided in Figure 4-2, and the A1 schematic diagram is contained in Figure 8-1. Inputs to this board include the 8-line data bus, the 5-line management bus (SRQ and EOI are terminated here), the Data Valid (DAV) handshake bus line, and the TTL DWL control line from the RF plug-in via the top (A2) PC assembly.

For purposes of description, this PC assembly can be divided into input-control, data-processing, and output-control logic circuits. The input-control logic consists of the Data-Input, Address Decoder, Management Bus Logic, Address Flip-Flop (FF), and Handshake Logic circuits. Of these circuits, the address flip-flop provides the primary input control. The current state of this bistable circuit determines whether or not the programmable logic array (PLA) is enabled. The state of this flip-flop can be synchronously controlled via a clock (DAV) pulse, or it can be controlled asynchronously via a clear (REN or IFC) pulse. Asynchronous control occurs whenever the controller sets either the REN line high (inactive) or the IFC line low (active). When either of these conditions occurs, flip-flop U17 changes to the unlisten state (Q=0, $\overline{Q}$=1). Synchronous (clocked) control of this flip-flop is provided by the DAV handshake line. A negative pulse on this line clocks U17 to a listen state (Q=1, $\overline{Q}$=0) when the U17 J-K inputs are at 1 and 0 respectively. The J-input of U17 is at a logic-level 1 when the sweep generator preset address has been decoded and the ATN line is active. Conversely, flip-flop U17 is clocked to the unlisten state when the J-input is 0 and the K-input is 1. The K-input goes to 1 whenever the PLA has decoded an ASCII ? (universal unlisten address command). During the periods when U17 has a logic-level 0 on both its J and K inputs, input clock pulses have no effect on the multivibrator output; the state of the flip-flop remains unchanged from its previously-set state.

The functions of the other input control circuits are as follows: the data-input logic (Schmitt trigger circuits) conditions the input data bits: the address decoder decodes the listen address data and sets the logic state of the MLA (my listen address) line; the management bus logic conditions and controls the ATN, REN, and IFC-bus management lines; and the handshake logic controls the logic states of handshake control lines NRFD and NDAC. The two conditions under which the handshake logic is enabled are: (1) when the ATN line is active or (2) when the address flip-flop is in the listen state. When the handshake logic is enabled, the active (low) state of the DAV line will cause the sweep generator to handshake (NRFD goes low (active) and NDAC goes high (inactive) approximately 10ns later) with the controller, except when TTL DWL is active (low). During oscillator bandswitch, TTL DWL goes active for several milliseconds to allow for oscillator settling time.

The data-processing logic is composed of the PLA, Mode Logic, Range Logic, V/E Decoder, and the Increment Generator. Of these circuits, the PLA is the primary data-processing device. The PLA has been programmed to set its output-circuit logic in accordance with logic conditions present in its input circuit. In effect, this device decodes the input-data lines and sets its output accordingly. As shown in Figure 4-2, the eight output lines are composed of increment (INC), mode (M), V or E (V/E), numerical digit ($\overline{\text{digit}}$), trigger (T), filter ($\overline{\text{F}}$), range (R), and unlisten (UNL) control lines. These control lines are routed to appropriate data-processing and/or output-control circuits. Each control line, along with the logic circuit it controls, is described in the paragraphs that follow.

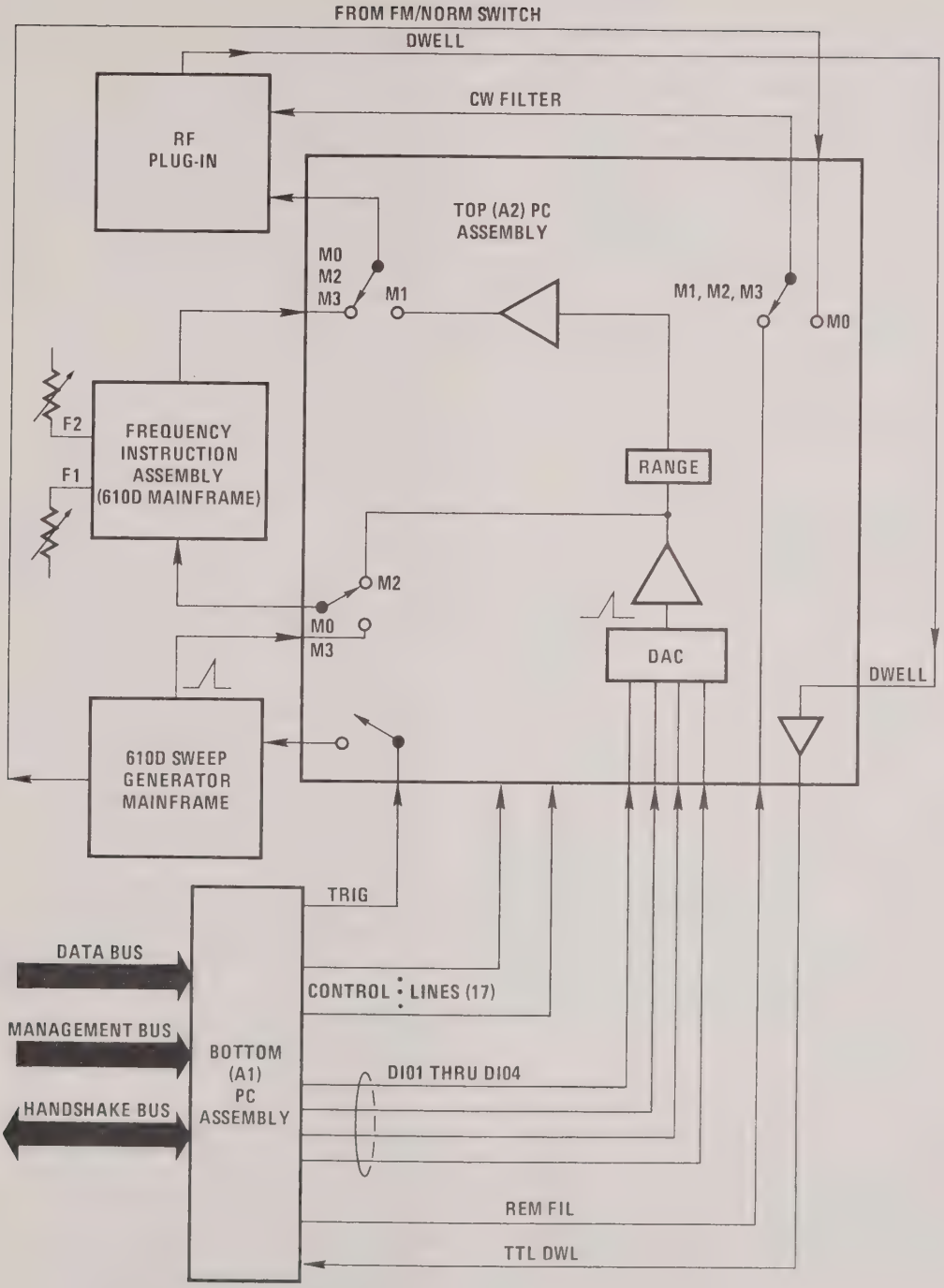


Figure 4-1. Functional Block Diagram, Option 16 GPIB Circuits

The M control line (pin 17) is set high as a result of the PLA decoding an ASCII M from the data bus. When this line goes high, it enables a latch circuit to respond to the next data byte transmitted over the data bus. The least-significant four bits of the next data byte (numerical data in BCD format) are stripped from the data bus and applied to a second mode-logic latch circuit. This latch supplies a two-bit binary number to a 2-4 decoder circuit. This decoder then completes the decoding of the mode information. Once decoded, the binary information that represents the operational mode is applied both as A1 Assembly output data and as present-mode feedback to the PLA input circuit.

The R control line (pin 11) goes high as a result of two separate input conditions: the PLA decodes ASCII R and the present-mode feedback lines indicate mode 1 or mode 2 operation. When this control line goes high, it, like the mode-logic circuit previously described, enables a latch circuit to respond to the next byte of data transmitted over the data bus. As described for the mode logic, the least-significant four bits are stripped from the data bus and applied to a second latch. The output of this latch is a three-bit binary number. Of this three-bit number, the two least-significant bits are applied to a 2-4 decoder and the most-significant bit is applied to an inverter. The outputs of these two circuits, decoder and inverter, are binary representations of the controller-selected range data.

The V/E control line (pin 12), like the R control line, goes high as a result of two separate input conditions: the PLA decodes an ASCII V or E and the present-mode feedback lines indicate mode 1 or mode 2 operation. When these two input conditions are met, the V/E control line enables a pair of NAND gates. These NAND gates further decode the V or E data and differentiate between the two codes. If the ASCII code is V, then the $\overline{V}$ line is set low. Conversely, if the ASCII code is not V, then the $\overline{E}$ line is set low. The $\overline{V}$ or $\overline{E}$ logic is applied to the shift register clock generator and to A1 Assembly output pins.

The INC line (pin 18), like the mode and range lines previously described, requires two separate input conditions before it will go high. These two input conditions are: the PLA decodes one of the increment codes (ASCII O, T, H, K) and the present-mode feedback lines indicate either mode 1 or mode 2 operation. (Decoding an ASCII T in mode 3 will result in a trigger.) When the INC line goes high, it enables the increment generator to further decode the data bus. The output of the increment generator (i.e., the logic state of the OINC, T, H, and K output lines) determines which frequency-point decade-digit is to be incremented.

The output-control logic is composed of the Shift Register Clock Generator (SRCG), Filter Control Logic, and Trigger Logic. Of these circuits, the SRCG is of primary importance. The output of this circuit, REG CK, is used to clock the data-bus frequency-point data (DIO 1 thru DIO 4) into shift registers located on the top (A2) PC assembly. The SRCG operates as a 4-count countdown circuit whose operation is controlled by the $\overline{V}$, $\overline{\text{digit}}$, DAVL, and $\overline{E}$ control lines. In capsule, this circuit loads a 4-count when $\overline{V}$ goes low, counts down each time a DAVL pulse is received, and resets either when a countdown of 4 is achieved or when $\overline{E}$ goes low. The remaining two output-control circuits, filter control logic and trigger logic, are described below.

Filter Control Logic. The filter control logic is controlled by the $\overline{F}$ control line (pin 13). This control line goes low as a result of two PLA input conditions: the PLA decodes an ASCII F and the present-mode feedback lines indicate mode 1, mode 2, or mode 3 operation. The output of this circuit, REM FIL, is used to control the CW filter in/out status. When the REM FIL line is high, the CW filter is inserted into the oscillator input circuit. Conversely, when this line is low, the filter is switched out of the oscillator input circuit.

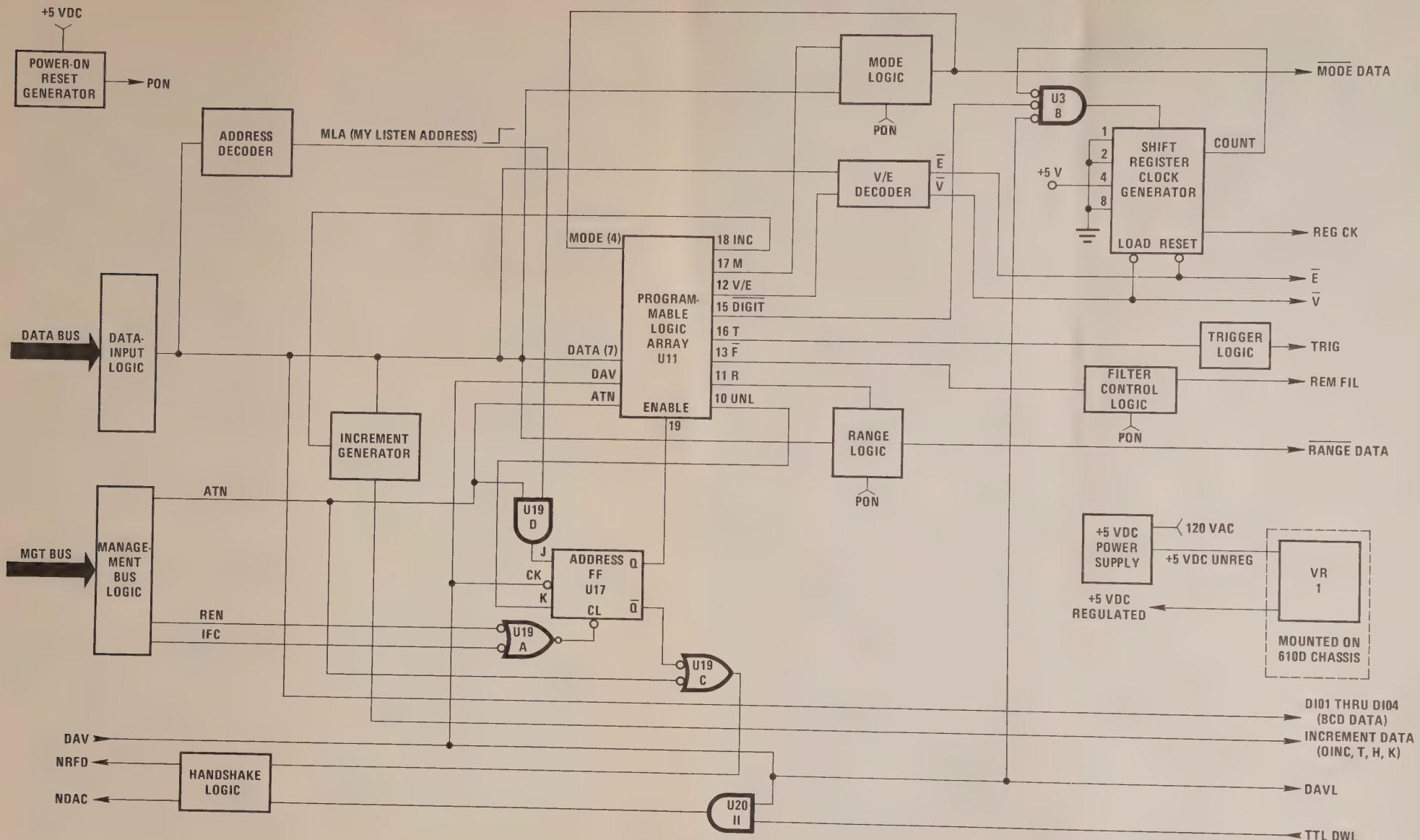


Figure 4-2. Functional Block Diagram, Bottom (A1) PC Assembly

Trigger Logic. The trigger logic is controlled by the T control line (pin 16). This control line goes high as a result of two PLA input conditions: the PLA decodes an ASCII T and the present-mode feedback lines indicate mode 3 operation. (An ASCII T decoded during mode 1 or mode 2 operation enables the increment generator.) When the T line goes high, the trigger-logic output goes high; when T returns to a low state, the trigger-logic output follows suit. This circuit action results in a positive pulse being impressed on the TRIG line when the trigger-logic circuit is activated.

Two functional circuits plus one PLA output line remain to be described. These circuits--which fall outside of the input-control, data-processing, and output-control circuit divisions--are described below.

UNL control line (pin 10). This control line, like most of the control lines already described, goes high as a result of two separate input conditions: the PLA decodes an ASCII? and the input condition of the ATN line is active (low). When the UNL control line goes high, it causes the address flip-flop, U17, to change to its unlisten ($Q=0$, $\overline{Q}=1$) state when clocked by a negative DAV pulse.

+5 Vdc Power Supply. This circuit, along with chassis-mounted voltage regulator VR1, provides the +5 Vdc integrated circuit and transistor Vcc voltages.

Power-On Reset Generator (PON). The PON circuit provides for the initialization of Option 16 logic circuits, inhibits the reception of data and control bits during initialization, and clears the listen flip-flop, U17, to its unlisten state ($Q=0$, $\overline{Q}=1$).

4-4. FUNCTIONAL DESCRIPTION, TOP PC ASSEMBLY (A2)

The A2 PC Assembly contains the digital-to-analog conversion and range selection circuits plus mode switching circuits that control the sweep generator output functions. A functional block diagram of this assembly is provided in Figure 4-3; the A2 schematic diagram is contained in Figure 8-2. For purposes of description, this PC assembly can be divided into three functional groups. These groups are: digital-to-analog converter (DAC) control and conversion circuits, range selection circuits, and operational-mode switching circuits. Functional descriptions of these circuits are provided in the following paragraphs.

DAC Control and Conversion Circuits. This group of circuits is composed of a 4-Stage Shift Register, a 4-Stage Counter/Latch, the DAC, and the DAC Operational Amplifier. The primary inputs for this group of circuits are the four data lines that are input to the 4-stage shift register. These are the same four lines (DIO 1 thru DIO 4) that were stripped from the A1 Assembly data bus, prior to the data bus being input to the PLA. These four lines contain numerical frequency-point data arranged in a BCD format. This BCD data is clocked into the first shift register (after the shift register has been reset by a $\overline{V}$ logic voltage) by the input REG CK pulse. When all of the available frequency-point data has been clocked into the shift registers, the data is transferred from the shift registers into corresponding counter/latch circuits, and concurrently applied to the DAC. The DAC converts this digital data into an analog current (I). The output of the DAC -- analog current -- is applied to an operational amplifier, converted to a voltage, and applied to both the range selector circuits and the mode switching circuits.

One other important set of inputs to this group of circuits are the INC DATA (increment) lines (OINC, T, H, and K). These lines, which are ANDed with the DAVL line, are used to increment the appropriate counter/latch circuit (units, tens, hundreds, or thousands).

Range Selector Circuits. This group of circuits is composed of five solid-state analog switches, nine potentiometers, and an operational amplifier circuit. The nine potentiometers include four potentiometer-

pairs used to set upper and lower frequency limits in ranges 1 thru 4 (R1 thru R4). The output of the potentiometer circuit is an analog voltage that represents a discrete frequency point within a preselected range of frequencies. This voltage is amplified by the operational amplifier and applied to the mode-switching circuits.

Mode-Switching Circuits. The mode-switching circuits are composed of five solid-state analog switches with their associated logic gates and a logic switch, which consists of three NAND gates and a transistor. As illustrated in Figure 4-3, the analog switch-contacts are controlled by the logic state of the $\overline{M1}$, $\overline{M2}$, and $\overline{M3}$ mode control lines. In the case of mode 0 and mode 3 operation, the circuit output to both the Frequency Instruction Board and to the RF plug-in is controlled by $\overline{M1}$ and $\overline{M2}$ combinational logic.

The other mode-switching functional block is the Filter Control Logic Switch. This circuit is an arrangement of logic components used to provide CW filter control. In mode 0 ($\overline{M\emptyset}$ line low), the logic-switch circuit provides for the in/out status of the filter to be controlled by the rear panel FM/NORM switch. In modes 1, 2, and 3 ($\overline{M\emptyset}$ line high), the logic-switch circuits provide for the in/out status of the filter to be controlled by the REM FIL control line.

Two additional circuits, contained within the A2 PC Assembly but not part of the circuit groups already described, are the Power Supply and the TTL DWL Operational Amplifier. The power supply is used to provide +/- 15Vdc, +13Vdc, and -3.3Vdc for the applicable A2 integrated circuits. The TTL DWL Operational Amplifier is used to amplify the dwell signal from the RF plug-in and to translate this analog voltage into a TTL logic level.

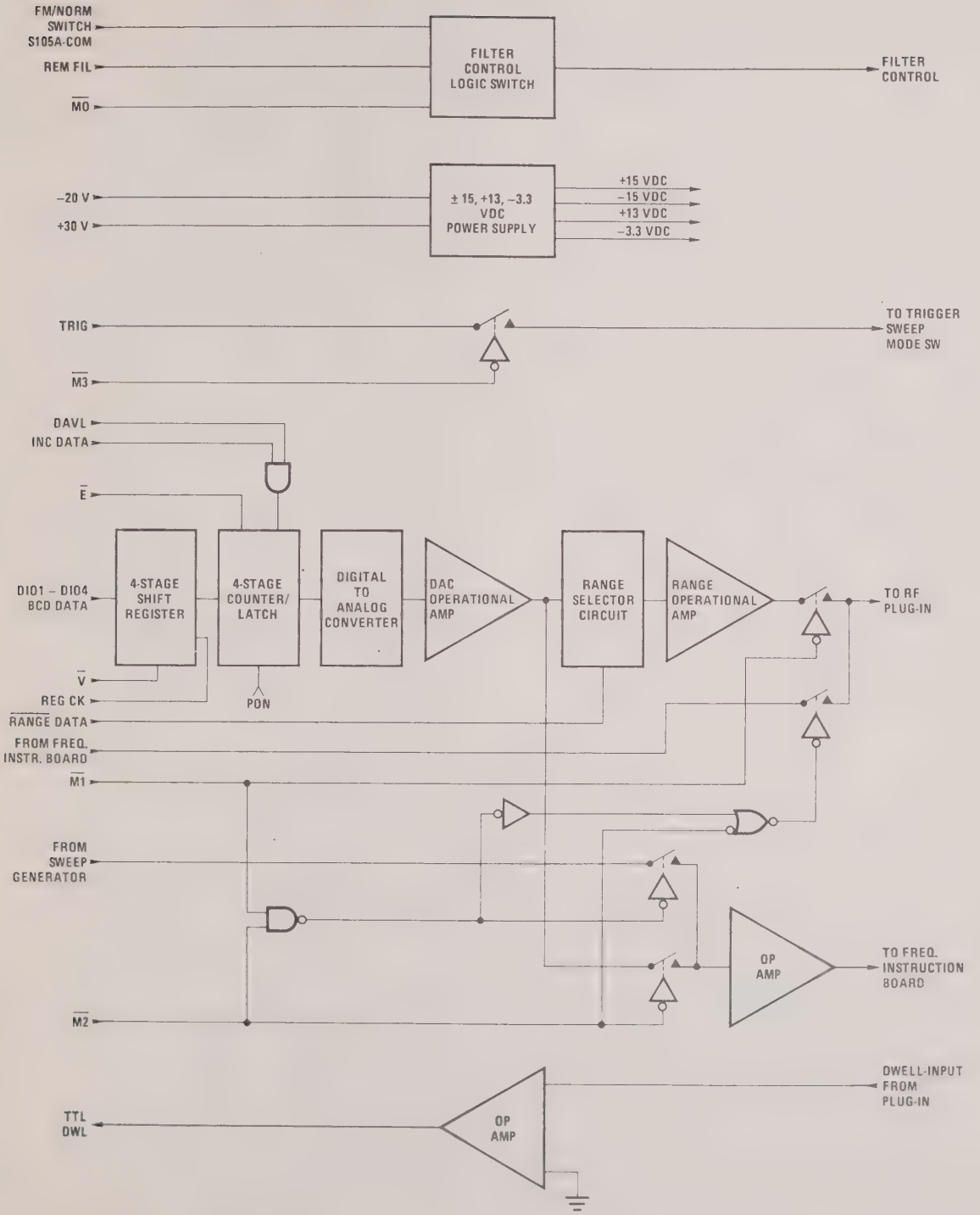


Figure 4-3. Functional Block Diagram, Top (A2) PC Assembly

SECTION V

PERFORMANCE VERIFICATION

5-1. INTRODUCTION

This section contains instructions for verifying the performance of the Model 610D/ Option 16 RF Sweep Generator's GPIB circuits. The instructions contained in this section are intended to provide a complete and thorough method of verifying that the sweep generator is responding to GPIB control.

5-2. PERFORMANCE VERIFICATION TESTS

The Performance Verification Test Procedure is contained in Table 5-2; equipment used to perform the test is illustrated in Figure 5-1. The performance verification procedure (Table 5-2) is functionally arranged in groups of tests so that it may be entered into at any point, and so that any group of tests may be performed individually. The procedure in Table 5-2 is constructed so that it will be compatible with any of the GPIB system controllers commonly in use. In the procedure, the ASCII command given for each procedural step is the command that the Option 16 circuits need to "see." In order for these commands to be placed on the bus, however, they have to be incorporated into a programming statement that the System Controller can use. An example of a BASIC (computer language) programming statement, as used by the Tektronix 4051, is: PRI@5: "M1RØFIVØE" (RETURN) (Sweep Generator address set to 5.)

5-3. TEST EQUIPMENT

Table 5-1 contains a listing of the recommended test equipment for performing the Performance Verification Test Procedure.

Table 5-1. Recommended Test Equipment

INSTRUMENT	REQUIRED CHARACTERISTICS	MANUFACTURER AND MODEL
COMPUTER/ CALCULATOR	IEEE 488 (IEC 625) GPIB Capability	TEKTRONIX 4051, HP 9825A, or COMMODORE-PET 2001
DIGITAL VOLTMETER	4 1/2-digit (minimum) voltage resolution	FLUKE 8600A, HP 3466A, or Equivalent
OSCILLOSCOPE	Vertical Sensitivity - 1mV	TEKTRONIX 5440 or Equivalent

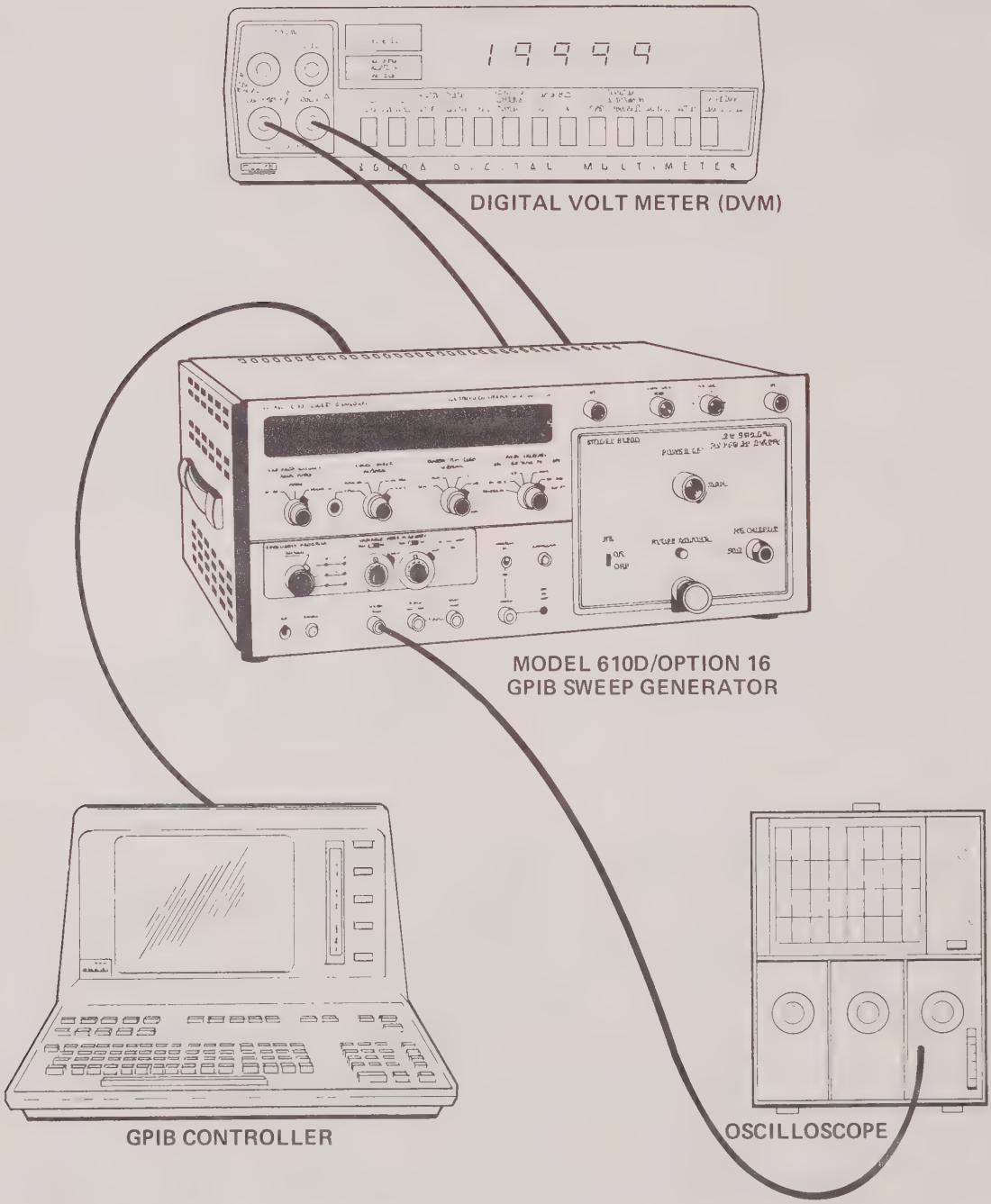


Figure 5-1. Performance Verification Test Setup

Table 5-2. Performance Verification Test Procedures (Page 1 of 6)

STEP	MONITOR POINT	ASCII COMMAND	PROCEDURE/INDICATION
1.	N/A	N/A	Remove both top and bottom dust covers. **CAUTION** Use extreme care to avoid damage to the sweep generator slide rule dial pointer mechanism. With the top cover removed, this mechanism is exposed and susceptible to damage and/or misalignment through mishandling.
2.	N/A	N/A	Position POWER switch to ON.
	Power Supply Voltage Tests		
			NOTE Reference voltage measurements to U4, pin 8 (chassis ground).
3.	U4, pin 16	N/A	DVM indicates +5.0 ± 0.2 Vdc.
4.	U18, pin 13	N/A	DVM indicates +15 ± 0.6 Vdc.
5.	U18, pin 4	N/A	DVM indicates -15.0 ± 0.6 Vdc.
			NOTE 1 Insure that an RF plug-in is installed in the 610D Mainframe. In order for the following test to be valid, the circuits that generate the frequency tuning voltages must be properly loaded.
			NOTE 2 The low-end and high-end slide rule dial calibration marks referred to in Mode 0, Mode 2, and Mode 3 tests are the two vertical dots that are located off-scale at either end of the slide rule dial.

Table 5-2. Performance Verification Test Procedure (Page 2 of 6)

STEP	MONITOR POINT	ASCII COMMAND	PROCEDURE/INDICATION
	Mode 0 Performance Tests		
			NOTE 1 In the following Mode 0 tests, no ASCII command is necessary. When initially energized, the sweep generator will come on-line in Mode 0 (MØ). NOTE 2 Reference voltage measurements to J401, pin 23.
6.	J401, pin 24	N/A	a. Position front panel controls as follows: SWEEP MODE - MANUAL FREQ SELECTOR - CW MKR b. While observing DVM, rotate the VAR . FREQ MKR control and verify that DVM voltage changes. DVM should indicate 0 ± 0.025 Vdc at the low-end calibration mark of the slide rule dial; this voltage should increase to 9.750 ± 0.025 Vdc at the high-end calibration mark.
7.	J401, pin 21	N/A	a. Position FM/NORM switch (rear panel) to FM. DVM should indicate +4.9 ± 0.5 Vdc. b. Position FM/NORM switch to NORM. DVM should indicate -15 ± 0.5 Vdc.
	Mode 1 Performance Tests		
8.	J401, pin 24	M1 RØ V0E	DVM indicates 0 ± 0.010 Vdc.
9.	Same as step 8.	V25ØØE	DVM indicates +2.437 ± 0.010 Vdc. (2.427 to 2.447 Vdc.)
10.	Same as step 8.	V5ØØØE	DVM indicates +4.875 ± 0.010 Vdc. (4.865 to 4.885 Vdc.)
11.	Same as step 8.	V75ØØE	DVM indicates +7.312 ± 0.010 Vdc. (7.302 to 7.322 Vdc.)

Table 5-2. Performance Verification Test Procedure (Page 3 of 6)

STEP	MONITOR POINT	ASCII COMMAND	PROCEDURE/INDICATION
12.	Same as step 8.	V9999E	DVM indicates +9.749 ± 0.010 Vdc. (9.739 to 9.759 Vdc). NOTE In steps 14 thru 17 and steps 34 thru 37, the resultant frequency-tuning voltages are derived by multiplying the number of frequency increments by the frequency tuning-ramp voltage value (9.75 Vdc).
13.	Same as step 8.	VØE	DVM indicates 0 Vdc (nominal).
14.	Same as step 8.	OOOOOOOOOO (ten X1 INC commands)	DVM indicates 0.009 Vdc (nominal). (Voltage increments by ≈ 9.75mV.)
15.	Same as step 8.	TTTTTTTTTT (ten X10 INC commands)	DVM indicates 0.107 Vdc (nominal). (Voltage incremented by ≈ 98mV.)
16.	Same as step 8.	HHHHHHHHH (nine X100 INC commands)	DVM indicates 0.985 Vdc (nominal). (Voltage increments by ≈ 878mV.)
17.	Same as step 8.	KKKKKKKK (eight X1000 INC commands)	DVM indicates 8.780 Vdc (nominal). (Voltage increments by ≈ 7.8 V.) CAUTION When touching the DVM test lead to the pins of A2J2, use care to avoid shorting pins together. Shorting these pins together could result in damage to A2 IC components.
18.	A2J2, pin 2 (top PC assembly)	N/A	DVM indicates TTL low (0 to +0.5 Vdc).
19.	Same as step 18.	R1	DVM indicates TTL high (+3.5 to +5.0 Vdc).

Table 5-2. Performance Verification Test Procedure (Page 4 of 6)

STEP	MONITOR POINT	ASCII COMMAND	PROCEDURE/INDICATION
20.	A2J2, pin 5.	N/A	DVM indicates TTL low (0 to +0.5 Vdc).
21.	Same as step 20.	R2	DVM indicates TTL high (+3.5 to +5.5 Vdc).
22.	A2J2, pin 6.	N/A	DVM indicates TTL low (0 to +0.5 Vdc).
23.	Same as step 22.	R3	DVM indicates TTL high (+3.5 to +5.5 Vdc).
24.	A2J2, pin 7	N/A	DVM indicates TTL low (0 to +0.5 Vdc).
25.	Same as step 24.	R4	DVM indicates TTL high (+3.5 to +5.0 Vdc).
26.	A2J2, pin 4	N/A	DVM indicates TTL low (0 to +0.5 Vdc).
27.	Same as step 26.	RØ	DVM indicates TTL high (+3.5 to +5.0 Vdc).
28.	J401, pin 21	FO	DVM indicates +4.9 Vdc (nominal).
29.	Same as step 28.	FI	DVM indicates -15 Vdc (nominal).
	Mode 2 Performance Tests		
30.	N/A	N/A	Position FREQ SELECTOR control to F1 TO F2.
31.	J401, pin 24	M2 VØE	While observing DVM, rotate F1 control and verify that DVM voltage readout changes. DVM voltage should indicate 0 ± 0.025 Vdc at low-end calibration mark of slide rule dial; this voltage should increase to +9.750 ± 0.025 Vdc at high-end calibration mark. Return F1 dial pointer to low-end calibration mark.
32.	Same as step 31.	V9999E	While observing DVM, rotate F2 control and verify that DVM voltage readout changes. DVM voltage should indicate +9.750 ± 0.025 Vdc at high-end calibration mark of slide rule dial; this voltage should decrease to 0 ± 0.025 Vdc at low-end calibration mark. Return F2 dial pointer to high-end calibration mark and adjust F2 control until DVM indicates exactly 9.750 Vdc.

Table 5-2. Performance Verification Test Procedure (Page 5 of 6)

STEP	MONITOR POINT	ASCII COMMAND	PROCEDURE/INDICATION
33.	Same as step 31.	VØE	Rotate F1 control until DVM indicates exactly 0.000 Vdc.
34.	Same as step 31.	OOOOOOOOOO (ten X1 INC commands)	DVM indicates 0.009 Vdc (nominal). (Voltage increments by ≈ 9.75mV.)
35.	Same as step 31.	TTTTTTTTTT (ten X10 INC commands)	DVM indicates 0.107 Vdc (nominal). (Voltage increments by ≈ 98mV.)
36.	Same as step 31.	HHHHHHHHH (nine X100 INC commands)	DVM indicates 0.985 Vdc (nominal). (Voltage increments by ≈ 878mV.)
37.	Same as step 31.	KKKKKKKK (eight X1000 INC commands)	DVM indicates 8.780 Vdc (nominal). (Voltage increments by ≈ 7.8 V.)
38.	J401, pin 21	FO	DVM indicates +4.9 Vdc (nominal).
39.	Same as step 38.	FI	DVM indicates -15 Vdc (nominal).
	Mode 3 Performance Tests		
40.	N/A	N/A	Position SWEEP MODE control to TRIG position. NOTE In step 41, position oscilloscope controls for operation in the external horizontal input mode.
41.	N/A	N/A	Connect Horizontal Input of oscilloscope to HORIZ OUT jack on sweep generator front panel.
42.	DVM: J401, pin 24 O'Scope: HORIZ OUT jack	M3T	Sweep generator initiates a voltage sweep when ASCII T is sent over the bus.
43.	N/A	N/A	Position FREQ SELECTOR control to CW MKR position.

Table 5-2. Performance Verification Test Procedure (Page 6 of 6)

STEP	MONITOR POINT	ASCII COMMAND	PROCEDURE/INDICATION
44.	Same as step 42.	N/A	Rotate VAR FREQ MKR control and verify that DVM voltage readout changes. DVM should indicate 0 Vdc at low-end calibration mark on slide rule dial; this voltage should increase to 9.75 Vdc (nominal) at high-end calibration mark.
45.	DVM: J401, pin 21	FO	DVM indicates +4.9 Vdc (nominal).
46.	N/A	N/A	Performance verification test is complete. Remove all test equipment and replace sweep generator dust covers.

SECTION VI

MAINTENANCE

6-1. INTRODUCTION

This section contains instructions for checking and adjusting the Model 610D RF Sweep Generator's Option 16 GPIB circuits, as well as information regarding the Option 16 PC assembly orientation and parts layout. The test and adjustment procedure is arranged so that it may be universally applied to any one of the different GPIB system-controller types presently in use, e.g. Tektronix 4051, HP 9825A, PET 2001, etc. The Option 16 PC Assembly orientation and component parts layouts are contained in Figures 6-1, 6-2, and 6-3.

6-1.1 General Maintenance

General maintenance requirements for working on the Option 16 PC assemblies are the same as would be applicable to any other electronic assemblies. The Option 16 PC assemblies are constructed of solid-state, bipolar and field-effect-transistor (FET) devices. Careful handling of electronic test leads when taking circuit measurements is essential in order to prevent component damage. Solid-state component junctions are easily damaged due to test lead "bridging" of Vcc voltages to voltage-sensitive pins.

6-1.2 Corrective Maintenance

Corrective maintenance consists of repairing and/or replacing defective components. If it becomes necessary to remove and replace PC assembly components, the following precautions should be observed. When replacing defective parts, use only a low-wattage (15W) or temperature-controlled (600 to 700° F) soldering iron. The use of either a higher wattage or a non-temperature-controlled soldering tool may result in damage to adjacent components and/or damage to circuit board traces. The A2 Assembly contains three FET switches. These switches are the three analog switches U16, U18, and U19. When replacing any of these switches, observe the following precautions: avoid contact with component leads, avoid touching component leads to ungrounded surfaces, and avoid working on these components with ungrounded tools. Ground the tip of the soldering iron before soldering component leads to the circuit board eyelets. These FET switches are extremely sensitive to static electricity, and are easily ruined by careless handling.

6-1.3 Test Equipment

A listing of recommended test equipment to be used in maintaining and servicing the sweep generator is contained in the Performance Verification section of this manual (Section V), Table 5-1.

6-2. TESTS AND ADJUSTMENTS

The test and adjustment procedure for the Option 16 circuitry is contained in Table 6-1. This procedure is written so that it will be compatible with any of the several types of calculator/computer systems commonly used as GPIB system controllers. The tests and/or adjustments specified in Table 6-1 will occur as a result of the Option 16 circuits "seeing" the associated ASCII command. The ASCII commands provided in this table are complete as written except for address and unaddress commands. The user is required to incorporate these ASCII commands into a programming statement that is compatible with the system controller used. An example of a properly-configured BASIC (computer language) programming statement for use with the Tektronix 4051 Graphic System, is: PRI@5: "M1R0VØE" (RETURN) (Sweep Generator address set to 5).

Table 6-1. Tests and Adjustments (Page 1 of 3)

STEP	ASCII COMMAND	PROCEDURE
		NOTE 1 Insure that an RF plug-in is installed in the 610D Mainframe. In order for the following adjustments to be valid, the digital-to-analog converter (DAC) circuits must be properly loaded. NOTE 2 These steps are meant to be followed sequentially. The ASCII command given for each procedural step must be prefaced by the sweep generator address numeral.
1.	N/A	Remove the top and bottom dust covers. CAUTION Use extreme care to avoid damage to the sweep generator's slide rule dial-pointer mechanism. With the top cover removed, this mechanism is exposed and susceptible to damage and/or misalignment through mishandling.
2.	N/A	Position front-panel SWEEP MODE control to MANUAL.
3.	N/A	Position front-panel POWER switch to ON.
Power Supply Voltage Tests		
		NOTE Reference voltage measurements to U4, pin 8 (chassis ground).
4.	N/A	Connect DVM to U4, pin 16; DVM indicates +5 ± 0.2 Vdc.
5.	N/A	Connect DVM to U18, pin 13; DVM indicates +15 ± 0.6 Vdc.
6.	N/A	Connect DVM to U18, pin 4; DVM indicates -15 ± 0.6 Vdc.

Table 6-1. Tests and Adjustments (Page 2 of 3)

STEP	ASCII COMMAND	PROCEDURE
	Mode 1 Calibration	
		NOTE Reference voltage measurements to J401, pin 23.
7.	M1 R0 VØE	Connect DVM to U18, pin 6. Adjust R7 for 0 ± 0.02 Vdc.
8.	V9999E	Adjust R9 for 11.2 ± 0.02 Vdc.
9.	VØE	Connect DVM to J401, pin 24. Adjust R34 for 0 ± 0.005 Vdc.
10.	V9999E	Adjust R16 for 9.75 ± 0.005 Vdc.
		NOTE In Steps 11 thru 18, the RNG 1 thru RNG 4 F1 and F2 potentiometers will be varied throughout their range to check their operational performance. Since each of these potentiometers has been previously set for a specific frequency point (refer to paragraph 3-6), record its present voltage value before rotating the adjustment screw. After performing all of the potentiometer operational checks in steps 11 thru 18, go back and readjust each potentiometer for its recorded value.
11.	R1 VØE	Rotate R17 adjustment screw throughout its range; verify that the voltage will adjust between 0 ± 0.02 Vdc and 9.75 ± 0.02 Vdc. Record this voltage and readjust R17 for 0 Vdc.
12.	V9999E	Rotate R18 adjustment screw throughout its range; verify that the voltage will adjust between 0 ± 0.02 Vdc and 9.75 ± 0.02 Vdc. Record this voltage and readjust for 9.75 Vdc.
13.	R2 VØE	Rotate R19 adjustment screw throughout its range; verify that the voltage will adjust between 0 ± 0.02 Vdc and 9.75 ± 0.02 Vdc. Record this voltage and readjust for 0 Vdc.

Table 6-1. Tests and Adjustments (Page 3 of 3)

STEP	ASCII COMMAND	PROCEDURE
14.	V9999E	Rotate R20 adjustment screw throughout its range; verify that the voltage will adjust between 0 ± 0.02 Vdc and 9.75 ± 0.02 Vdc. Record this voltage and readjust R20 for 9.75 Vdc.
15.	R3 VØE	Rotate R21 adjustment screw throughout its range; verify that the voltage will adjust between 0 ± 0.02 Vdc and 9.75 ± 0.02 Vdc. Record this voltage and readjust R21 for 0 Vdc.
16.	V9999E	Rotate R22 adjustment screw throughout its range; verify that the voltage will adjust between 0 ± 0.02 Vdc and 9.75 ± 0.02 Vdc. Record this voltage and readjust R22 for 9.75 Vdc.
17.	R4 VØE	Rotate R23 adjustment screw throughout its range; verify that the voltage will adjust between 0 ± 0.02 Vdc and 9.75 ± 0.02 Vdc. Record this voltage and readjust R23 for 0 Vdc.
18.	V9999E	Rotate R24 adjustment screw throughout its range; verify that the voltage will adjust between 0 ± 0.02 Vdc and 9.75 ± 0.02 Vdc. Record this voltage and readjust R24 for 9.75 Vdc.
19.	R1 VØE	Readjust R17 to the voltage value recorded in step 11.
20.	V9999E	Readjust R18 to the voltage value recorded in step 12.
21.	R2 VØE	Readjust R19 to the voltage value recorded in step 13.
22.	V9999E	Readjust R20 to the voltage value recorded in step 14.
23.	R3 VØE	Readjust R21 to the voltage value recorded in step 15.
24.	V9999E	Readjust R22 to the voltage value recorded in step 16.
25.	R4 VØE	Readjust R23 to the voltage value recorded in step 17.
26.	V9999E	Readjust R24 to the voltage value recorded in step 18.
27.	N/A	The Option 16 circuit calibration procedure is now complete. Disconnect all test equipment and replace dust covers.

6-3. TROUBLESHOOTING

A troubleshooting chart listing trouble symptoms and their probable cause(s) is provided in Table 6-2.

Table 6-2. Troubleshooting Chart (Page 1 of 2)

SYMPTOM	ISOLATION PROCEDURE AND/OR PROBABLE CAUSE
1. Sweep generator will not operate in Mode 0 (MØ).	a. Remove connector J1 from top (A2) PC assembly and connect jumper between the following pins: 6 and 7, 9 and 10, 11 and 12. b. If normal operation is restored, check the following IC's: A2U23, A2U18, and A2U17. c. If normal operation is not restored, malfunction is in the sweep generator mainframe and not in the Option 16 circuitry.
2. Sweep generator operates normally in Mode 0, but will not operate in Modes 1, 2, or 3.	a. Examine GPIB interconnect cable and check for broken wires and/or damaged connections. b. Check address switches S1 thru S5 and insure that sweep generator is set to the correct address.
3. Sweep generator operates normally in Mode 1 Range 0, but one or more of its remaining ranges (R1 thru R4) cannot be selected and/or adjusted.	a. Potentiometers associated with malfunctioning range(s) defective. b. One or more of the following IC's defective: A2U19, A2U16, A1U13, A1U12.
4. CW filter will not respond to bus programming.	a. One or more of the following IC's defective: A2U20, A1U7, A1U4, A1U15. b. Transistor A2Q1 defective.
5. Sweep generator will not respond to GPIB trigger command.	a. Sweep generator not in Mode 3. b. SWEEP MODE control not in TRIG position. c. EXTERNAL TRIGGER ADJ potentiometer (R148) on mainframe PC assembly part number 610D-ML-835 improperly adjusted. d. IC A2U16 defective.

Table 6-2. Troubleshooting Chart (Page 2 of 2)

SYMPTOMS	ISOLATION PROCEDURE AND/OR PROBABLE CAUSE
6. No +5 Vdc at A2U4, pin 16.	a. Fuse A1F1 blown. b. Voltage regulator IC, VR1, defective. c. One or more rectifier diode(s), A1CR1 thru A1CR4, defective. d. Transformer A1T1 defective.
7. No +15 Vdc at A2U18, pin 13.	a. Check mainframe connector J1, pin 3, for +30 Vdc. (J1 connects to P1 on Option 16 top (A2) PC assembly.) If +30 Vdc not present, power supply in Model 610D Mainframe defective. b. IC A2U22 defective.
8. No -15 Vdc at A2U18, pin 4.	a. Check mainframe connector J1, pin 4, for -20 Vdc. (J1 connects to P1 on Option 16 top (A2) PC assembly.) If -20 Vdc not present, power supply in Model 610D Mainframe defective. b. IC A2U21 defective.
9. No +13 Vdc at A2U23, pin 7.	a. Diode A2CR5 defective. b. IC A2U23 defective.
10. No -3 Vdc at A2U23, pin 4.	a. Diode A2CR6 defective. b. IC A2U23 defective.

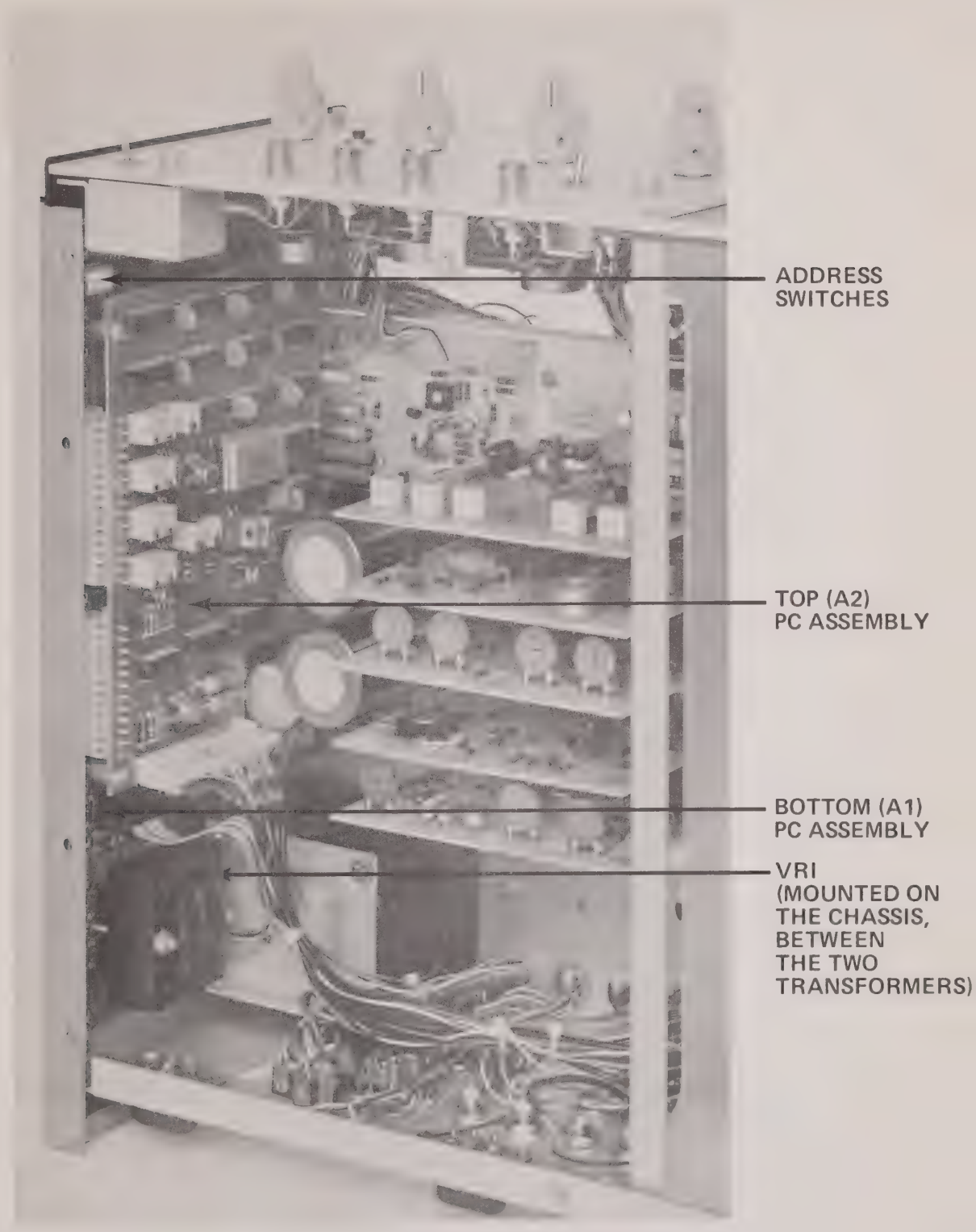


Figure 6-1. Orientation of Option 16 PC Assemblies, within the Model 610D Mainframe

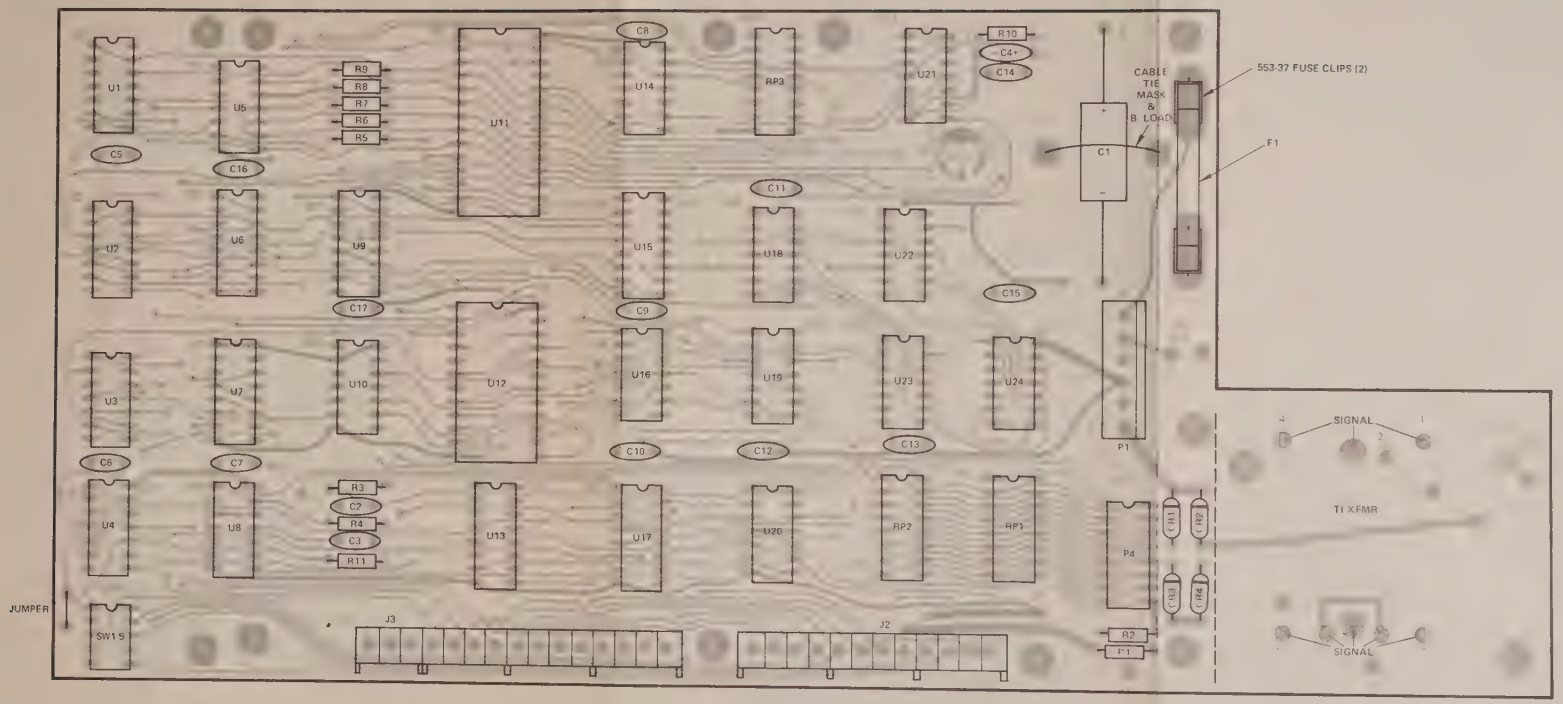


Figure 6-2. Bottom (A1) PC Assembly, Parts Layout

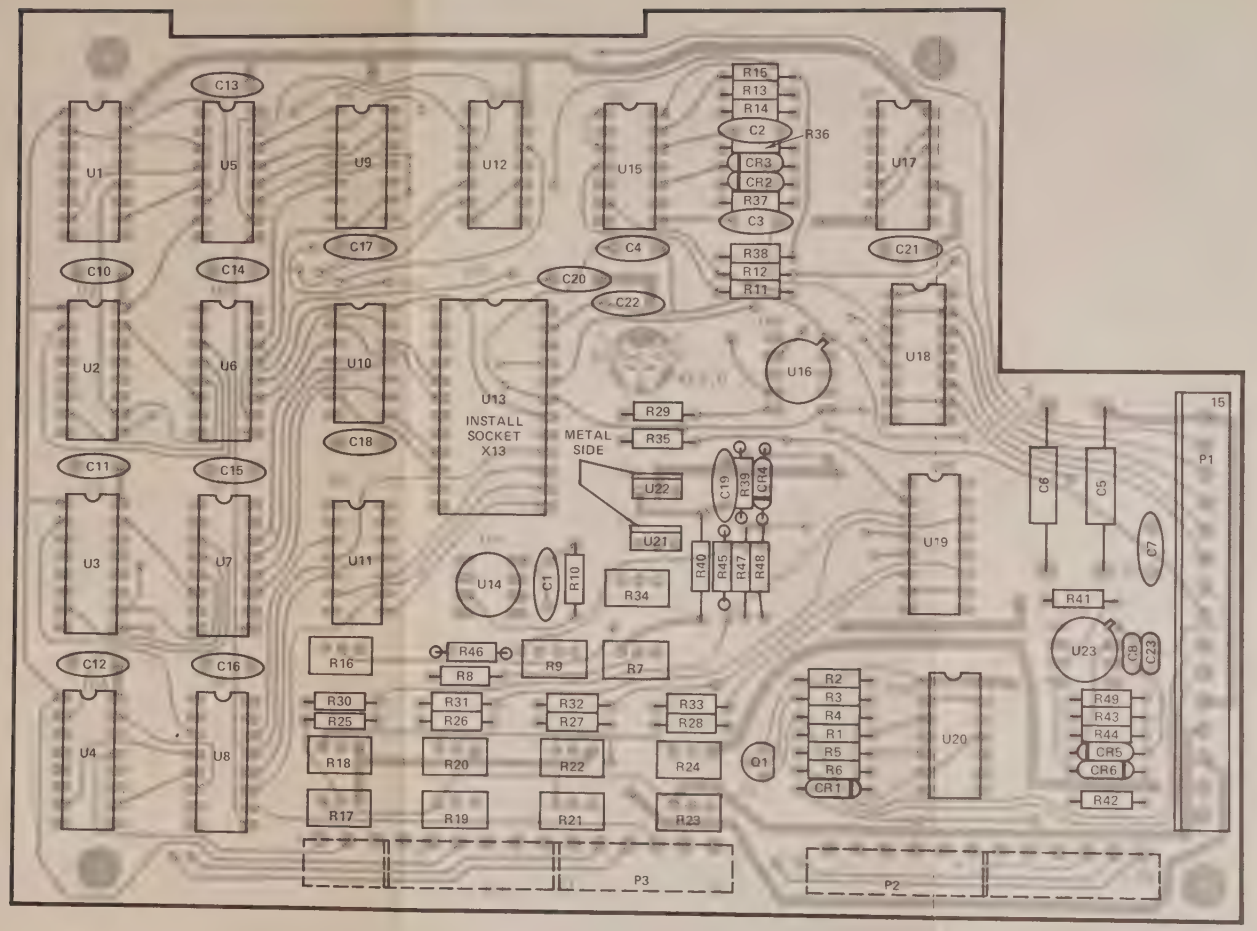


Figure 6-3. Top (A2) PC Assembly, Parts Layout

SECTION VII

PARTS LISTS

7-1. GENERAL

This section contains the parts lists for the Option 16 circuits contained within the Model 610D RF Sweep Generator. Included in each parts list are the reference designator, part description, and WILTRON part number for each item on each schematic. Items such as machined parts, chassis, and hardware are not included; these parts may, however, be ordered from WILTRON by special request.

7-2. PARTS LIST ABBREVIATIONS

Explanation of the abbreviations which appear in these parts lists are as follows:

CC - Carbon Composition
MF - Metal Film
PLA - Programmable Logic Array

7-3. ORDERING REPLACEABLE PARTS

Replaceable parts may be ordered either through your local representative or directly from:

WILTRON Company
825 East Middlefield Road
Mountain View, California 94043

Telephone: (415) 969-6500
TWX: 910-379-6578

When placing your order, give complete information, including the Model and Serial Number of the instrument, the full part description, WILTRON Part Number, and the quantity required.

7-4. PARTS LISTS

The parts lists are organized by P.C. board and subassembly (See Table 7-1).

Table 7-1. Replaceable Parts List (1 of 6)

REF. DES.	WILTRON PART NO.	DESCRIPTION
		OPTION 16, BOTTOM PC BOARD ASSEMBLY - 610-L-6100-3 (A1)
A1C1	250-71	Capacitor: Electrolytic, 2200μF, 25V
A1C2	220-470	Capacitor: Dipped Mica, 470pF
A1C3	220-130	Capacitor: Dipped Mica, 130pF
A1C4	250-14	Capacitor: Tantalum, 4.7μF, 10V
A1C5	230-4	Capacitor: Disc Ceramic, .01μF
A1C6	230-4	Capacitor: Disc Ceramic, .01μF
A1C7	230-4	Capacitor: Disc Ceramic, .01μF
A1C8	230-4	Capacitor: Disc Ceramic, .01μF
A1C9	230-4	Capacitor: Disc Ceramic, .01μF
A1C10	230-4	Capacitor: Disc Ceramic, .01μF
A1C11	230-4	Capacitor: Disc Ceramic, .01μF
A1C12	230-4	Capacitor: Disc Ceramic, .01μF
A1C13	230-4	Capacitor: Disc Ceramic, .01μF
A1C14	230-4	Capacitor: Disc Ceramic, .01μF
A1C15	230-4	Capacitor: Disc Ceramic, .01μF
A1C16	230-4	Capacitor: Disc Ceramic, .01μF
A1C17	230-4	Capacitor: Disc Ceramic, .01μF
A1CR1	10-SI2	Diode: Silicon
A1CR2	10-SI2	Diode: Silicon
A1CR3	10-SI2	Diode: Silicon
A1CR4	10-SI2	Diode: Silicon
A1F1	631-7	Fuse: 3AG 0.3A
A1J2	551-130	Connector: Molex, 12-Pin, Jack
Part Of A1J3	551-130	Connector: Molex, 12-Pin, Jack
Part Of A1J3	551-129	Connector: Molex, 3-Pin, Jack
A1P1	551-99	Connector: Molex, 6-Pin Indexed PC Board Mount
A1P4	553-69	Socket: 16-Pin, DIP
A1R1	110-3.32k-1	Resistor: MF, 3.32k, 1/4W, 1%
A1R2	110-6.81k-1	Resistor: MF, 6.81k, 1/4W, 1%
A1R3	110-1.18k-1	Resistor: MF, 1.18k, 1/4W, 1%
A1R4	110-10k-1	Resistor: MF, 10k, 1/4W, 1%
A1R5	110-3.83k-1	Resistor: MF, 3.83k, 1/4W, 1%
A1R6	110-3.83k-1	Resistor: MF, 3.83k, 1/4W, 1%
A1R7	110-3.83k-1	Resistor: MF, 3.83k, 1/4W, 1%
A1R8	110-3.83k-1	Resistor: MF, 3.83k, 1/4W, 1%
A1R9	110-3.83k-1	Resistor: MF, 3.83k, 1/4W, 1%
A1R10	110-10k-1	Resistor: MF, 10k, 1/4W, 1%

Table 7-1. Replaceable Parts List (2 of 6)

REF. DES.	WILTRON PART NO.	DESCRIPTION
A1R11	110-825-1	Resistor: MF, 825, 1/4W, 1%
A1RP1	123-2	Resistor: Array, 3.3k
A1RP2	123-3	Resistor: Array, 6.8k
A1RP3	123-2	Resistor: Array, 3.3k
A1S1-5	430-72	Switch, 5-Position, DIP
A1T1	320-46	Transformer: Signal
A1U1	54-74LS20	IC: Dual NAND Gate
A1U2	54-74LS04	IC: HEX Inverter
A1U3	54-74LS27	IC: Triple NOR Gate
A1U4	54-74LS08	IC: Quad AND Gate
A1U5	54-74LS260	IC: Dual NOR Gate
A1U6	54-74LS192	IC: Counter
A1U7	54-74LS109	IC: Dual J-$\overline{K}$ Flip-Flop
A1U8	54-74LS122	IC: One-Shot
A1U9	54-74LS109	IC: Dual J-$\overline{K}$ Flip-Flop
A1U10	54-7438	IC: Quad NAND D.C.
A1U11	54-19	IC: PLA, Programmed Per Spec-S-6110, Rev. 3
A1U12	54-74116	IC: Dual 4-Bit D Flip-Flop
A1U13	54-74LS139	IC: Dual 2-4 Decoder
A1U14	54-74LS04	IC: HEX Inverter
A1U15	54-74LS139	IC: Dual 2-4 Decoder
A1U16	54-74LS04	IC: HEX Inverter
A1U17	54-74LS112	IC: Dual J-$\overline{K}$ Flip-Flop
A1U18	54-74LS266	IC: Quad EX-NOR Gate
A1U19	54-74LS08	IC: Quad AND Gate
A1U20	54-74LS132	IC: Quad NAND Schmitt Trigger Inverter
A1U21	54-74LS132	IC: Quad NAND Schmitt Trigger Inverter
A1U22	54-74LS266	IC: Quad EX-NOR Gate
A1U23	54-74LS132	IC: Quad NAND Schmitt Trigger Inverter
A1U24	54-74LS132	IC: Quad NAND Schmitt Trigger Inverter

Table 7-1. Replaceable Parts List (3 of 6)

REF. DES.	WILTRON PART NO.	DESCRIPTION
		OPTION 16, TOP P.C. BOARD ASSEMBLY - 610-L-6101-3 (A2)
A2C1	220-100	Capacitor: Dipped Mica, 100pF
A2C2	220-330	Capacitor: Dipped Mica, 330pF
A2C3	220-330	Capacitor: Dipped Mica, 330pF
A2C4	230-32	Capacitor: Ceramic, .033μF
A2C5	250-34	Capacitor: Electrolytic, 10μF, 63V
A2C6	250-34	Capacitor: Electrolytic, 10μF, 63V
A2C7	230-4	Capacitor: Ceramic, .01μF, 500V
A2C8	230-30	Capacitor: Ceramic, .001μF, 500V
A2C9	230-4	Capacitor: Ceramic, .01μF, 500V
A2C10	230-4	Capacitor: Ceramic, .01μF, 500V
A2C11	230-4	Capacitor: Ceramic, .01μF, 500V
A2C12	230-4	Capacitor: Ceramic, .01μF, 500V
A2C13	230-4	Capacitor: Ceramic, .01μF, 500V
A2C14	230-4	Capacitor: Ceramic, .01μF, 500V
A2C15	230-4	Capacitor: Ceramic, .01μF, 500V
A2C16	230-4	Capacitor: Ceramic, .01μF, 500V
A2C17	230-4	Capacitor: Ceramic, .01μF, 500V
A2C18	230-4	Capacitor: Ceramic, .01μF, 500V
A2C19	230-4	Capacitor: Ceramic, .01μF, 500V
A2C20	230-4	Capacitor: Ceramic, .01μF, 500V
A2C21	230-4	Capacitor: Ceramic, .01μF, 500V
A2C22	230-4	Capacitor: Ceramic, .01μF, 500V
A2C23	230-30	Capacitor: Ceramic, .001μF, 500V
A2CR1	10-1N4446	Diode: Silicon
A2CR2	10-1N4446	Diode: Silicon
A2CR3	10-1N962B	Diode: Zener, 11V, 5%, 0.4W
A2CR4	10-1N4446	Diode: Silicon
A2CR5	10-1N4743A	Diode: Zener, 13V, 5%, 1W
A2CR6	10-1N746A	Diode: Zener, 3.3V, 5%, 1W
A2P1	551-112	Connector: Molex, Male, 15-Pin
A2P2	551-99	Connector: Molex, Male, 6-Pin (2 needed)
P/O A2P3*	551-99	Connector: Molex, Male, 6-Pin
P/O A2P3*	551-26	Connector: Molex, Male, 3-Pin
A2Q1	20-2N2907	Transistor
A2R1	101-5.1k-5	Resistor: CC, 5.1k, 1/4W, 5%
A2R2	101-5.1k-5	Resistor: CC, 5.1k, 1/4W, 5%
A2R3	101-51k-5	Resistor: CC, 51k, 1/4W, 5%
A2R4	101-5.1k-5	Resistor: CC, 5.1k, 1/4W, 5%
A2R5	101-2.94k-1	Resistor: MF, 2.94k, 1/4W, 1%
A2R6	101-3.83k-1	Resistor: MF, 3.83k, 1/4W, 1%

* A2P3 is composed of 2 each 551-99 and 1 each 551-26 connectors.

Table 7-1. Replaceable Parts List (4 of 6)

REF. DES.	WILTRON PART NO.	DESCRIPTION
A2R7	157-10kA	Potentiometer: CERMET, 15T, 10k
A2R8	110-1M-1	Resistor: MF, 1M, 1/4W, 1%
A2R9	157-5kA	Potentiometer: CERMET, 15T, 5k
A2R10	110-6.81k-1	Resistor: MF, 6.81k, 1/4W, 1%
A2R11	110-49.9k-1	Resistor: MF, 49.9k, 1/4W, 1%
A2R12	110-215k-1	Resistor: MF, 215k, 1/4W, 1%
A2R13	110-75k-1	Resistor: MF, 75k, 1/4W, 1%
A2R14	110-38.3k-1	Resistor: MF, 38.3k, 1/4W, 1%
A2R15	110-26.1k-1	Resistor: MF, 26.1k, 1/4W, 1%
A2R16	157-100kA	Resistor: Var., Cermet, 15T, 100k
A2R17	157-100kA	Resistor: Var., Cermet, 15T, 100k
A2R18	157-100kA	Resistor: Var., Cermet, 15T, 100k
A2R19	157-100kA	Resistor: Var., Cermet, 15T, 100k
A2R20	157-100kA	Resistor: Var., Cermet, 15T, 100k
A2R21	157-100kA	Resistor: Var., Cermet, 15T, 100k
A2R22	157-100kA	Resistor: Var., Cermet, 15T, 100k
A2R23	157-100kA	Resistor: Var., Cermet, 15T, 100k
A2R24	157-100kA	Resistor: Var., Cermet, 15T, 100k
A2R25	110-150k-1	Resistor: MF, 150k, 1/4W, 1%
A2R26	110-150k-1	Resistor: MF, 150k, 1/4W, 1%
A2R27	110-150k-1	Resistor: MF, 150k, 1/4W, 1%
A2R28	110-150k-1	Resistor: MF, 150k, 1/4W, 1%
A2R29	110-100k-1	Resistor: MF, 100k, 1/4W, 1%
A2R30	110-100k-1	Resistor: MF, 100k, 1/4W, 1%
A2R31	110-100k-1	Resistor: MF, 100k, 1/4W, 1%
A2R32	110-100k-1	Resistor: MF, 100k, 1/4W, 1%
A2R33	110-100k-1	Resistor: MF, 100k, 1/4W, 1%
A2R34	157-10kA	Resistor: Var., Cermet, 15T, 10k
A2R35	110-1M-1	Resistor: MF, 1M, 1/4W, 1%
A2R36	101-1k-5	Resistor: CC, 1k, 1/4W, 5%
A2R37	110-200k-1	Resistor: MF, 200k, 1/4W, 1%
A2R38	110-82.5k-1	Resistor: MF, 82.5k, 1/4W, 1%
A2R39	101-51k-5	Resistor: CC, 51k, 1/4W, 5%
A2R40	102-220-5	Resistor: CC, 220, 1/2W, 5%
A2R41	101-510-5	Resistor: CC, 510, 1/4W, 5%
A2R42	101-510-5	Resistor: CC, 510, 1/4W, 5%
A2R43	110-2.94k-1	Resistor: MF, 2.94k, 1/4W, 1%
A2R44	110-2.94k-1	Resistor: MF, 2.94k, 1/4W, 1%
A2R45	101-4.3M-5	Resistor: CC, 4.3M, 1/4W, 5%
A2R46	101-4.3M-5	Resistor: CC, 4.3M, 1/4W, 5%
A2R47	101-4.3M-5	Resistor: CC, 4.3M, 1/4W, 5%
A2R48	101-4.3M-5	Resistor: CC, 4.3M, 1/4W, 5%
A2R49	110-147-1	Resistor: MF, 147, 1/4W, 1%
A2U1	54-74LS175	IC: Quad D Flip-Flop
A2U2	54-74LS175	IC: Quad D Flip-Flop
A2U3	54-74LS175	IC: Quad D Flip-Flop
A2U4	54-74LS175	IC: Quad D Flip-Flop

Table 7-1. Replaceable Parts List (5 of 6)

REF. DES.	WILTRON PART NO.	DESCRIPTION
A2U5	54-74LS160	IC: Decade Counter
A2U6	54-74LS160	IC: Decade Counter
A2U7	54-74LS160	IC: Decade Counter
A2U8	54-74LS160	IC: Decade Counter
A2U9	54-74LS04	IC: HEX Inverter
A2U10	54-74LS04	IC: HEX Inverter
A2U11	54-74LS04	IC: HEX Inverter
A2U12	54-74LS32	IC: Quad OR Gate
A2U13	60-9	IC: 4-Digit BCD D/A Converter
A2U14	50-LM308	IC: Operational Amplifier
A2U15	54-RC4136	IC: Quad Operational Amplifier
A2U16	50-DG200BA	IC: Dual Analog Switch
A2U17	54-74LS00	IC: Quad NAND Gate
A2U18	54-24	IC: Quad Analog Switch
A2U19	54-20	IC: Quad Analog Switch
A2U20	54-74LS38	IC: Quad NAND Gate, Open Collector
A2U21	54-MC7915	IC: -15V Regulator
A2U22	54-MC7815	IC: +15 Regulator
A2U23	54-LM308	IC: Operational Amplifier
A2X13	553-67	Socket: 24-Pin DIP

Table 7-1. Replaceable Parts List (6 of 6)

REF. DES.	WILTRON PART NO.	DESCRIPTION
		Chassis and Other Non-PC Board-Mounted Parts
TS2	701-2	Tip Point: 5-Pin
VR1	54-MC7805CP	+5V Regulator
None	553-70	Connector: 16-Pin DIP
None	553-71	Connector Clip
None	553-72	Connector (Rear Panel Bus Connector)
None	553-72A	Mounting Hardware
None	551-35	Connector Pins: Molex, Female
None	551-103	Housing for Crimp Terminals: Molex, 6-Pin
None	551-111	Housing for Crimp Terminals: Molex, 15-Pin

SECTION VIII

DIAGRAMS

8-1. GENERAL

This section contains the schematic diagrams for the two Model 610D/Option 16 printed circuit (PC) assemblies, plus an overall timing diagram of the General Purpose Interface Bus.

Table 8-1. List of Diagrams

Figure	Title	Page
8-1	Schematic Diagram, Bottom (A1) PC Assembly	8-3/8-4
8-2	Schematic Diagram, Top (A2) PC Assembly	8-5/8-6
8-3	Timing Diagram, General Purpose Interface Bus	8-7/8-8

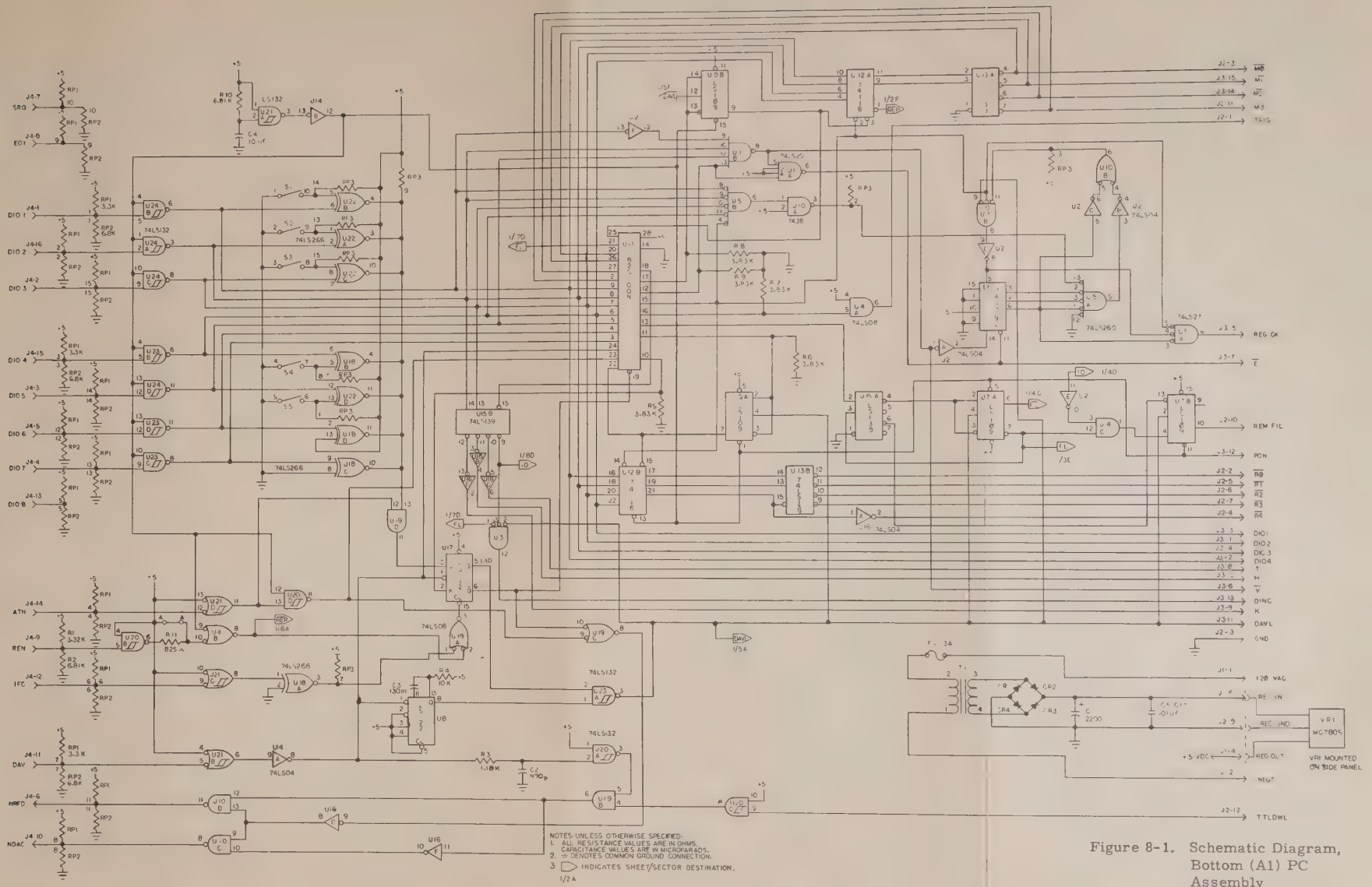
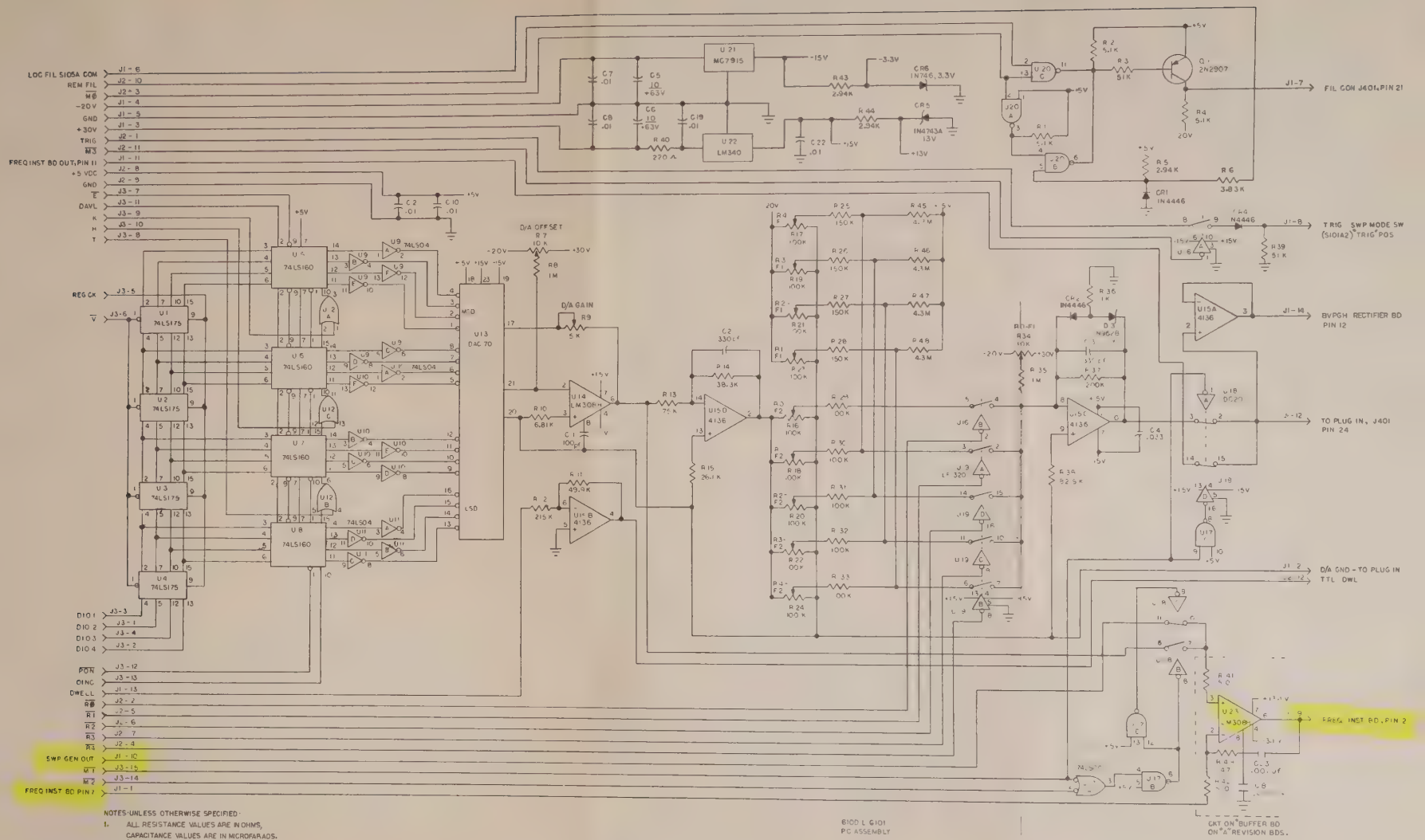


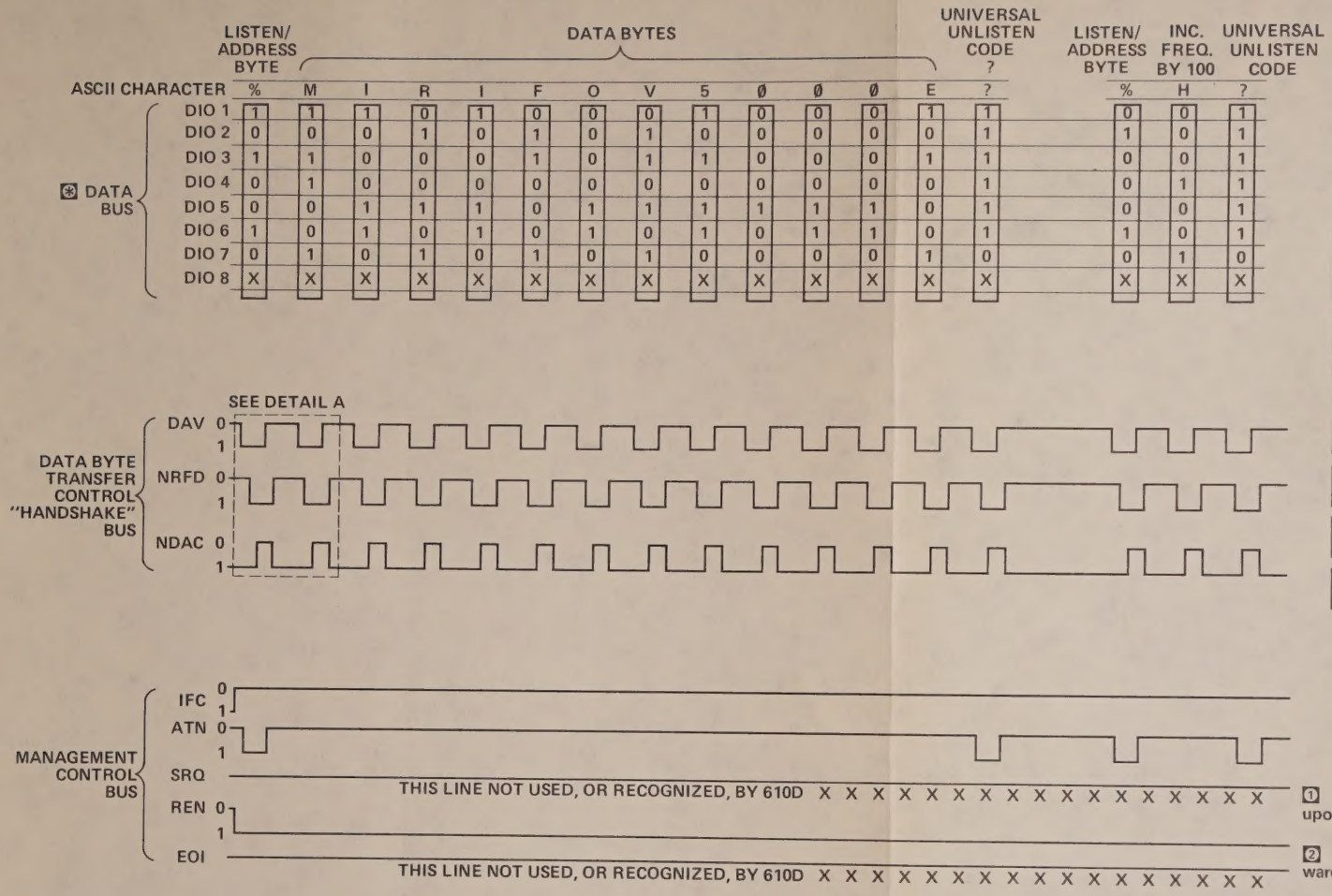
Figure 8-1. Schematic Diagram, Bottom (A1) PC Assembly (610D-Opt. 16-A1)

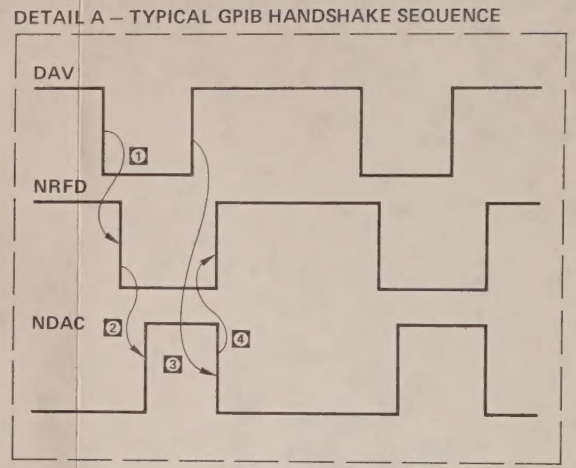


NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS.
2. ⏚ DENOTES COMMON GROUND CONNECTION.
3. ▷ INDICATES SHEET/SECTOR DESTINATION. 1/2A

Figure 8-2. Schematic Diagram, Top (A2) PC Assembly (610D-Opt. 16-A2)


LISTEN/ ADDRESS BYTE
DATA BYTES
UNIVERSAL UNLISTEN CODE
LISTEN/ ADDRESS BYTE
INC. FREQ. BY 100
UNIVERSAL UNLISTEN CODE
ASCII CHARACTER
% M I R I F O V 5 Ø Ø Ø E ?
% H ?
DATA BUS
DIO 1 1 1 1 0 1 0 0 0 1 0 0 0 1 1
DIO 2 0 0 0 1 0 1 0 1 0 0 0 0 0 1
DIO 3 1 1 0 0 0 1 0 1 1 0 0 0 1 1
DIO 4 0 1 0 0 0 0 0 0 0 0 0 0 0 1
DIO 5 0 0 1 1 1 0 1 1 1 1 1 1 0 1
DIO 6 1 0 1 0 1 0 1 0 1 0 1 1 0 1
DIO 7 0 1 0 1 0 1 0 1 0 0 0 0 1 0
DIO 8 X X X X X X X X X X X X X X
SEE DETAIL A
DATA BYTE TRANSFER CONTROL "HANDSHAKE" BUS
DAV 0 1
NRFD 0 1
NDAC 0 1
MANAGEMENT CONTROL BUS
IFC 0 1
ATN 0 1
SRQ
THIS LINE NOT USED, OR RECOGNIZED, BY 610D X X X X X X X X X X X X X X X X
REN 0 1
EOI
THIS LINE NOT USED, OR RECOGNIZED, BY 610D X X X X X X X X X X X X X X X X



NOTES

1. This response by NRFD to DAV going low is variable and depends upon the speed at which the 610D can respond to the data.

2. This response by NDAC to NRFD going low is forced by hardware.

3. This response by NDAC to DAV going high is forced by hardware. When DAV goes high it indicates that valid data is no longer on the bus.

4. This response by NRFD to NDAC going low is variable and depends upon the speed at which the LISTENER can process the accepted data.

This data represents a typical byte-serial, bit-parallel transfer of data to the Model 610D RF Sweep Generator. These two data strings are in ASCII code and they provide the 610D with the following information. 1st Data String: Listen Address = 5, Mode = Mode 1, Range = Range 1, CW Filter = Filter Out, Frequency = 5000th point (N=5000), Universal Unaddress Code (610D goes into idle). 2nd Data String: Listen Address = 5, Increment Frequency = 100 points ($X10^2$), Universal Unaddress Code (610D goes into idle).

Figure 8-3. Timing Diagram, General Purpose Interface Bus

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